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1-Mbps QUAD DIGITAL ISOLATORS

Check for Samples: ISO7240A, ISO7241A, ISO7242A

FEATURES

- 4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}
  - UL 1577 , IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- Typical 25-Year Life at Rated Working Voltage (See Application Note (SLLA197) and Figure 10)
- High Electromagnetic Immunity (See Application Report (SLLA181))
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

See the Product Notification section. The ISO7240A, ISO7241A and ISO7242A are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.
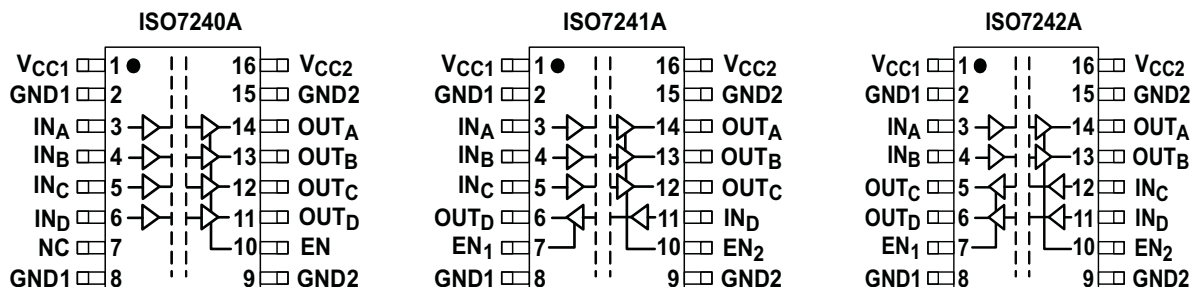
The ISO7240A has all four channels in the same direction while the ISO7241A has three channels the same direction and one channel in opposition. The ISO7242A has two channels in each direction.

The devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (See ISO7240CF (SLLS869) or contact TI for a logic low failsafe option).

These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.
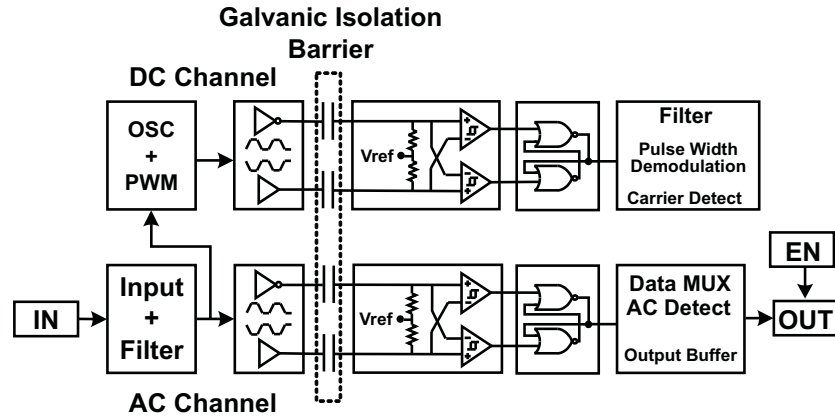
ISO7240A
ISO7241A
ISO7242A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

Table 1. Device Function Table ISO724x [1]

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER[1]
ISO7240ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	4/0	ISO7240A	ISO7240ADW (rail)
					ISO7240ADWR (reel)
ISO7241ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	3/1	ISO7241A	ISO7241ADW (rail)
					ISO7241ADWR (reel)
ISO7242ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	2/2	ISO7242A	ISO7242ADW (rail)
					ISO7242ADWR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

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ISO7240A
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ISO7242A

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ABSOLUTE MAXIMUM RATINGS[1]

				VALUE	UNIT
V_{CC}	Supply voltage[2], V_{CC1}, V_{CC2}			−0.5 to 6	V
V_I	Voltage at IN, OUT, EN			−0.5 to 6	V
I_O	Output current			±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	±1	
			All pins		
		Machine Model	ANSI/ESDS5.2-1996	±200	V
T_J	Maximum junction temperature			170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage[1], V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		−4			mA
t_{ui}	Input pulse width	ISO724xA	1			µs
$1/t_{ui}$	Signaling rate	ISO724xA	0		1000	kbps
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO724xA	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)		0		0.8	V
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
    For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

IEC 60747-5-2 INSULATION CHARACTERISTICS[1]

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	V
		Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	>10^9	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

ISO7240A
ISO7241A
ISO7242A

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ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V[(1)] OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
		1 Mbps			1	3	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		1 Mbps					
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		1 Mbps			10	16	
I_{CC2}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		1 Mbps			16	22	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		1 Mbps			13	20	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		1 Mbps			10	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		μA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.8$			V
			$I_{OH} = -20$ μA, See Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1			0.4	V
			$I_{OL} = 20$ μA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current			−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4$ sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
    For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		95	ns
PWD	Pulse-width distortion[(1)] $\|t_{PHL} - t_{PLH}\|$				10	
$t_{sk(o)}$	Channel-to-channel output skew [(2)]				2	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μs

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
		1 Mbps				1	3	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
		1 Mbps						
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			10	16	mA
		1 Mbps				10	16	
I_{CC2}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			9.5	15	mA
		1 Mbps				10	15	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	13	mA
		1 Mbps				8	13	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6	10	mA
		1 Mbps				6	10	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	ISO7240A	$V_{CC} - 0.4$			V
				ISO724x (5-V side)	$V_{CC} - 0.8$			
			$I_{OH} = -20$ µA, See Figure 1		$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1				0.4	V
			$I_{OL} = 20$ µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin (4E6\pi t)$			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
    For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		100	ns
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$				11	
$t_{sk(o)}$	Channel-to-channel output skew [2]				3	ns
				0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ISO7240A
ISO7241A
ISO7242A

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ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		0.5	1	mA
		1 Mbps			1	2	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		1 Mbps			4	7	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA
		1 Mbps			6	10	
I_{CC2}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		1 Mbps			16	22	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		1 Mbps			13	20	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		1 Mbps			10	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at V_{CC}, Single channel		0		µA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1 — ISO7240A	$V_{CC} - 0.4$			V
			$I_{OH} = -4$ mA, See Figure 1 — ISO724x (5-V side)	$V_{CC} - 0.8$			
			$I_{OH} = -20$ µA, See Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1			0.4	V
			$I_{OL} = 20$ µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin(4E6\pi t)$		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
     For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		100	ns
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$				11	
$t_{sk(o)}$	Channel-to-channel output skew [2]				2.5	ns
			0		1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V[(1)] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		0.5	1	mA
		1 Mbps			1	2	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		1 Mbps			4	7	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA
		1 Mbps			6	10	
I_{CC2}	ISO7240A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		9.5	15	mA
		1 Mbps			10	15	
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
		1 Mbps			8	13	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA
		1 Mbps			6	10	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.4$			V
			$I_{OH} = -20$ µA, See Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1			0.4	V
			$I_{OL} = 20$ µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4$ sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/µs

(1)   For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
       For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
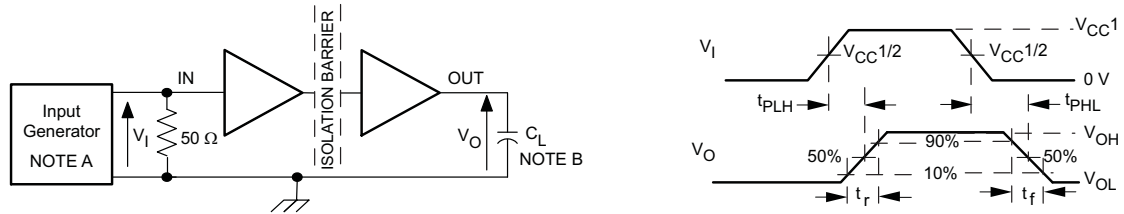
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	45		110	ns
PWD	Pulse-width distortion $|t_{PHL} - t_{PLH}|$[(1)]				12	
$t_{sk(o)}$	Channel-to-channel output skew [(2)]				3.5	ns
				0	1	
t_r	Output signal rise time	See Figure 1		2		
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1)   Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the
       same direction while driving identical specified loads.

ISO7240A
ISO7241A
ISO7242A

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PARAMETER MEASUREMENT INFORMATION

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

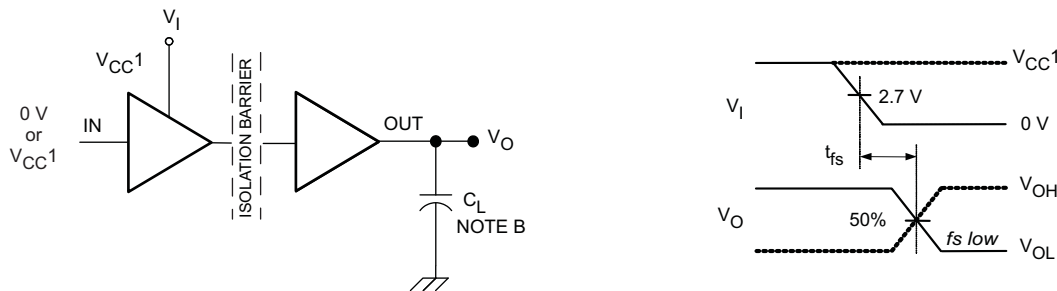**Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms**
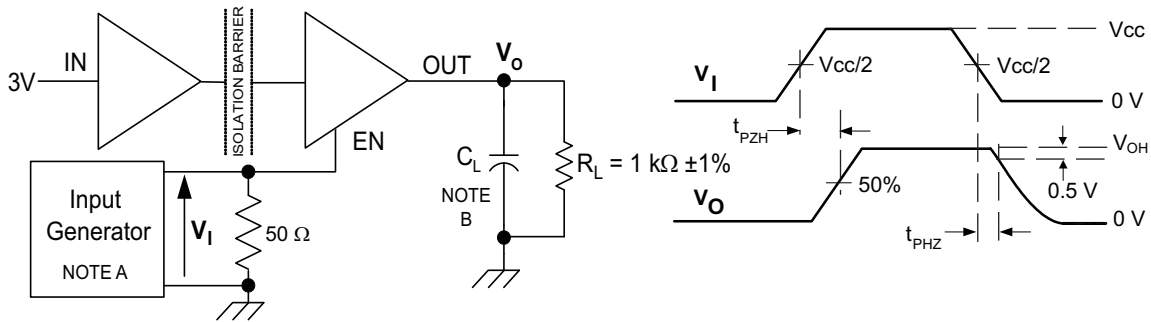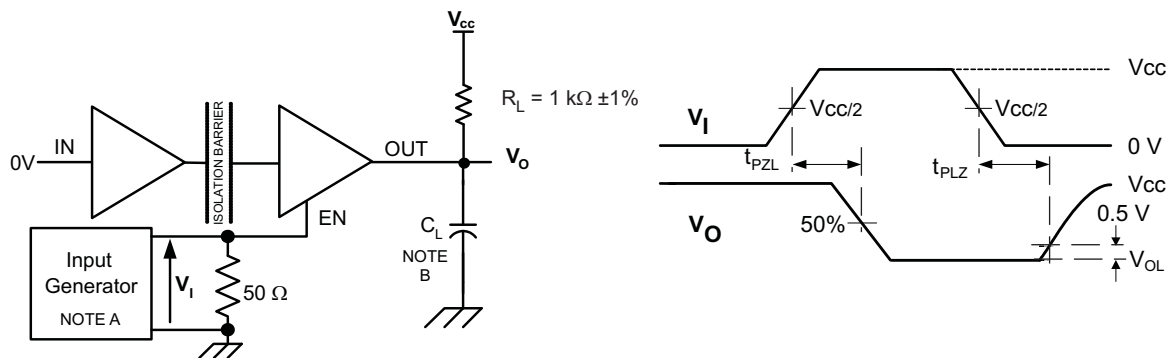
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

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PARAMETER MEASUREMENT INFORMATION (continued)

A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms
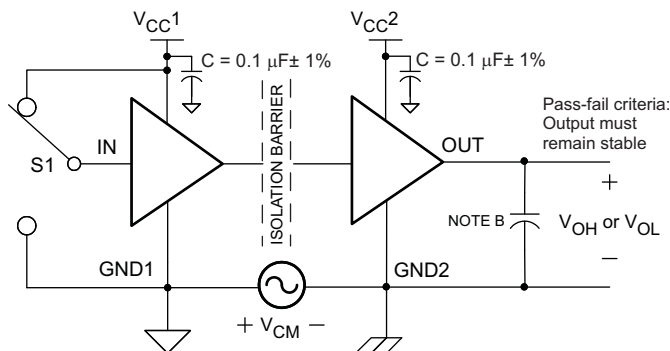
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform

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DEVICE INFORMATION

PACKAGE CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
C_{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)			2	pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			2	pF

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program[1]
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

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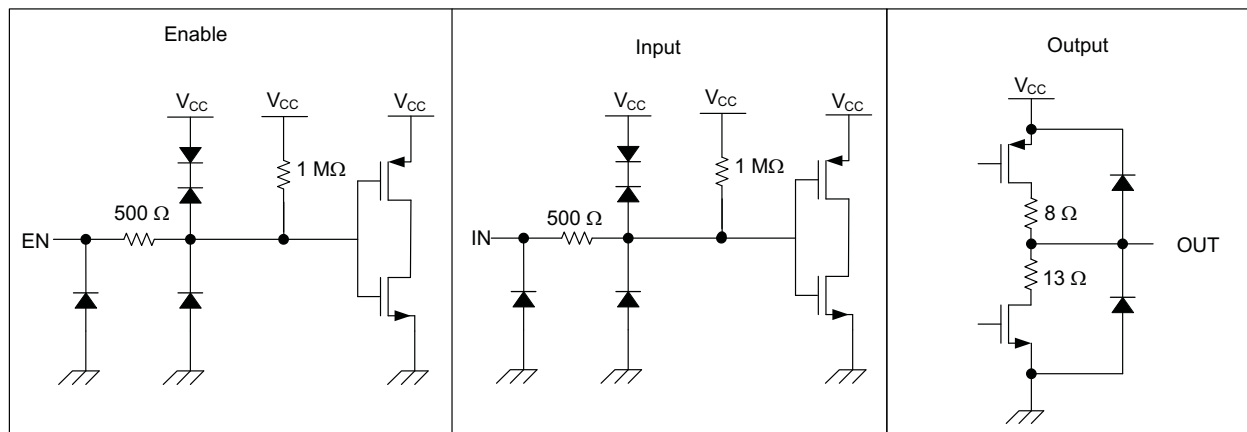
THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance[1]		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, Input a 50% duty cycle square wave			220	mW

(1)   Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES
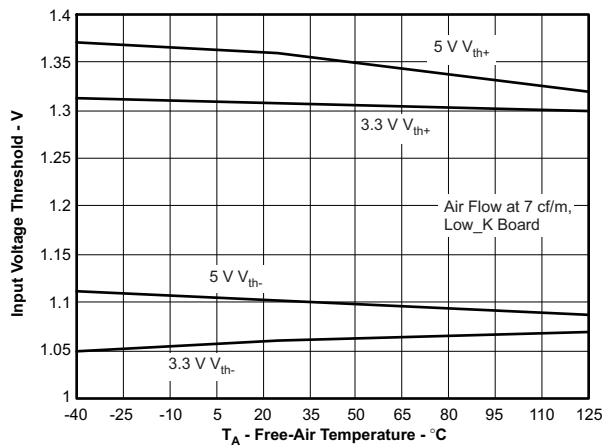
INPUT VOLTAGE THRESHOLD
vs
FREE-AIR TEMPERATURE

Figure 5.

V$_{CC1}$ FAILSAFE THRESHOLD
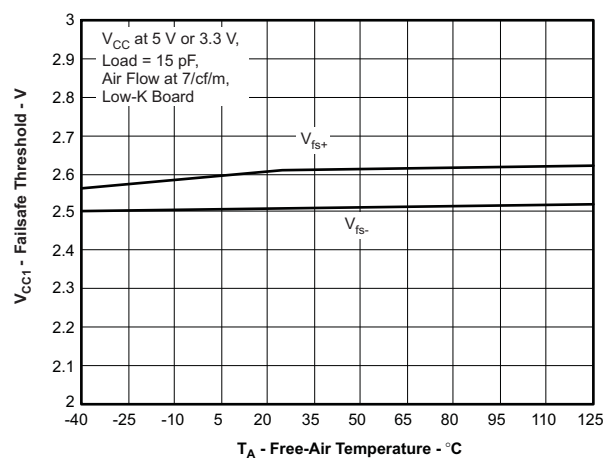**vs**
FREE-AIR TEMPERATURE

Figure 6.

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE
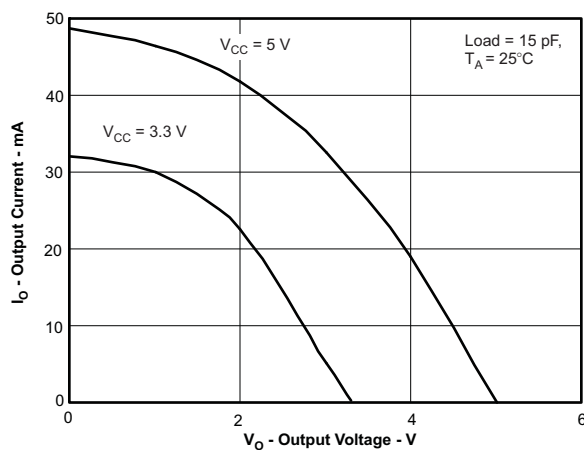
Figure 7.

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

Figure 8.

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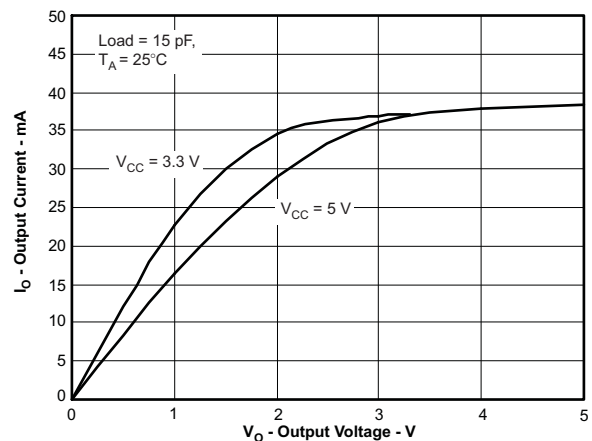SLLS905E – MAY 2008 – REVISED JANUARY 2010

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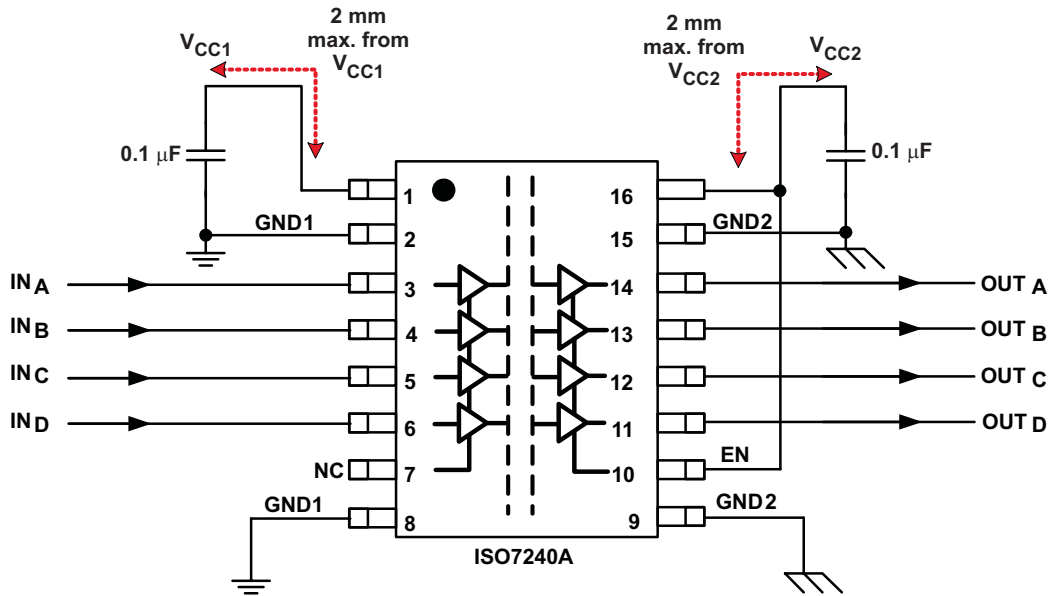
APPLICATION INFORMATION

Figure 9. Typical ISO7240A Application Circuit

LIFE EXPECTANCY vs. WORKING VOLTAGE
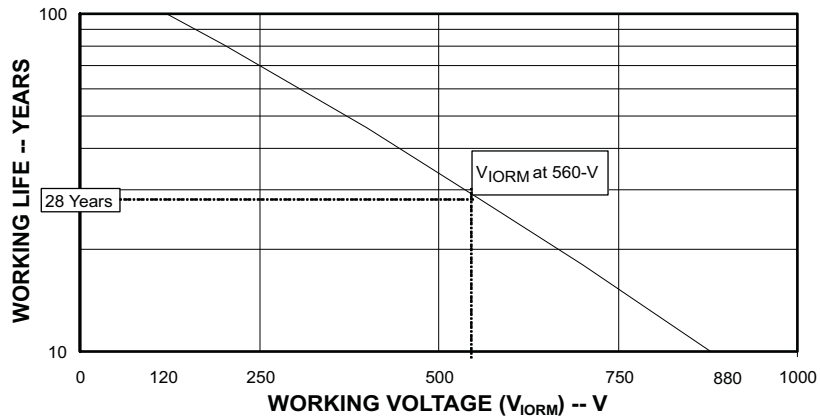
Figure 10. Time-Dependant Dielectric Breakdown Testing Results

Product Folder Link(s): *ISO7240A ISO7241A ISO7242A*

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ISO7242A

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PRODUCT NOTIFICATION

An ISO724xA anomaly occurs when a negative-going pulse below the specified 1 μs minimum bit width is input to the device. The output locks in a logic-low condition until the next rising edge occurs after a 1 μs period.

Positive noise edges in pulses of less than the minimum specified 1 μs have no effect on the device, and are properly filtered.

To prevent noise from interfering with ISO724xA performance, it is recommended that an appropriately sized capacitor be placed on each input of the device
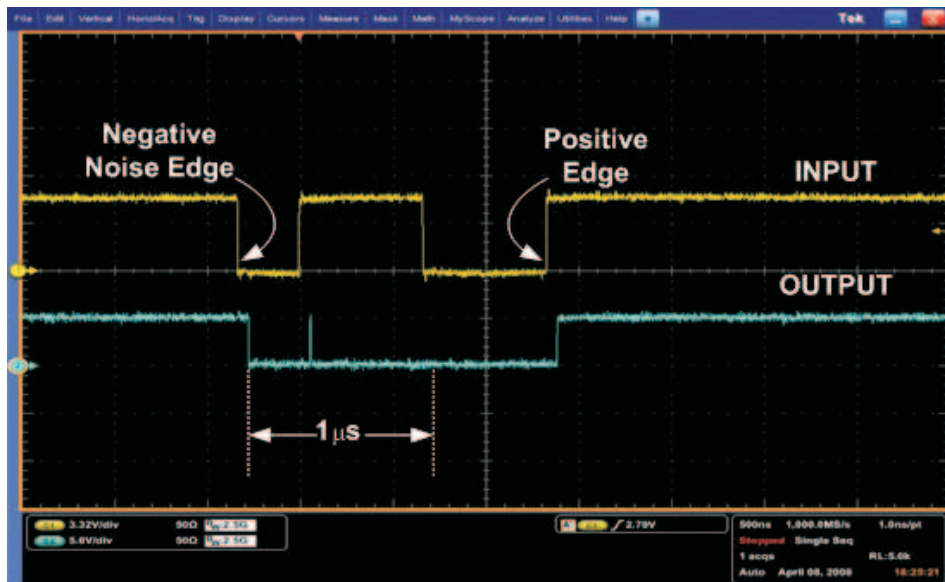

Figure 11. ISO724xA Anomaly

REVISION HISTORY

Changes from Original (May 2008) to Revision A   **Page**

- Changed In the PACKAGE CHARACTERISTICS table, line 1, change $L_{(IO1)}$ MIN value from 7.7mm to 8.34mm. 10

Changes from Revision A (July 2008) to Revision B   **Page**

- Added information to the 1st Feature bullet to include CSA and IEC 60950-1 certification 1
- Changed Figure 9 From: 20mm max.from V_{CCx} To: 2mm max. from V_{CCx}. 12

Changes from Revision B (December 2008) to Revision C   **Page**

- Changed I_{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA 4
- Changed I_{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA 5

Changes from Revision C (March 2009) to Revision D   **Page**

- Changed The Input circuit in the DEVICE I/O SCHEMATICS illustration. 10

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Changes from Revision D (December 2009) to Revision E   **Page**

- Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table 3
- Added C_{TI} - Tracking resistance (comparative tracking index to the PACKAGE CHARACTERISTICS table 10
- Added the IEC 60664-1 RATINGS TABLE 10

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ISO7240ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ISO7241A :

• Enhanced Product: ISO7241A-EP

NOTE: Qualified Version Definitions:

   • Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240ADWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO7241ADWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO7242ADWR	SOIC	DW	16	2000	358.0	335.0	35.0

DW (R–PDSO–G16)   PLASTIC SMALL OUTLINE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⌖ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040000–2/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS–013 variation AA.

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DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55   14x1,27

16x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around
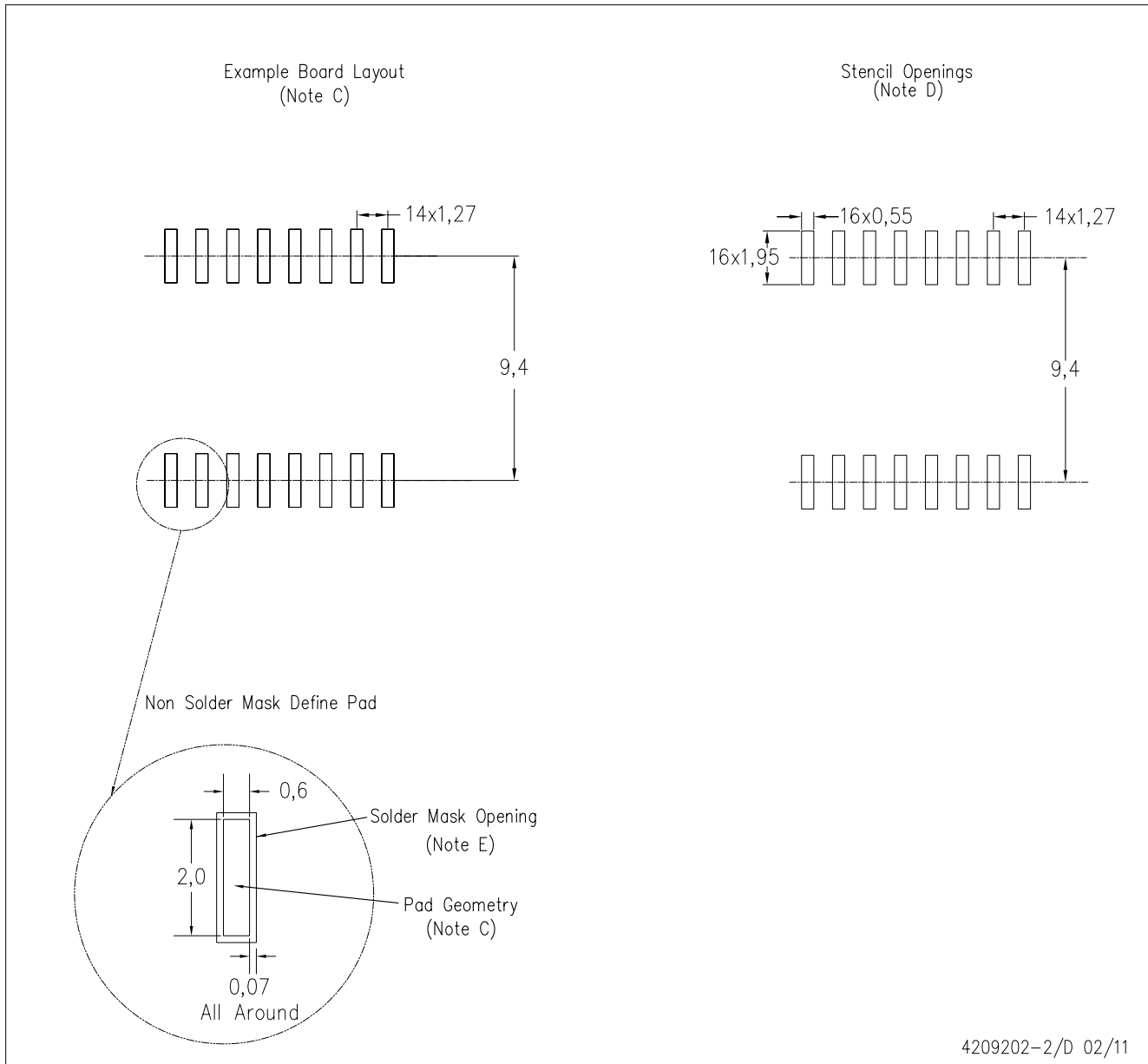
4209202−2/D 02/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Refer to IPC7351 for alternate board design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RF/IF and ZigBee® Solutions	www.ti.com/lprf		

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