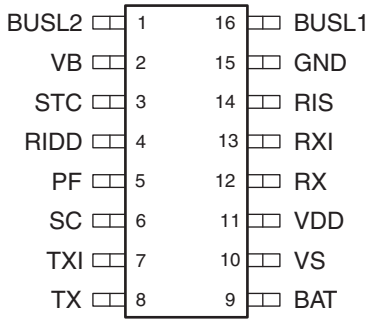
METER-BUS TRANSCEIVER

Check for Samples: TSS721A

FEATURES

- **Meter-Bus Transceiver (for Slave) Meets Standard EN1434-3**
- **Receiver Logic With Dynamic Level Recognition**
- **Adjustable Constant-Current Sink via Resistor**
- **Polarity Independent**
- **Power-Fail Function**
- **Module Supply Voltage Switch**
- **3.3-V Constant Voltage Source**
- **Remote Powering**
- **Up to 9600 Baud in Half Duplex for UART Protocol**
- **Slave Power Support**
  - **Supply From Meter-Bus via Output VDD**
  - **Supply From Meter-Bus via Output VDD or From Backup Battery**
  - **Supply From Battery – Meter-Bus Active for Data Transmission Only**

D PACKAGE
(TOP VIEW)



DESCRIPTION

TSS721A is a single chip transceiver developed for Meter-Bus standard (EN1434-3) applications.

The TSS721A interface circuit adjusts the different potentials between a slave system and the Meter- Bus master. The connection to the bus is polarity independent and supports full galvanic slave isolation with optocouplers.

The circuit is supplied by the master via the bus. Therefore, this circuit offers no additional load for the slave battery. A power-fail function is integrated.

The receiver has dynamic level recognition, and the transmitter has a programmable current sink.

A 3.3-V voltage regulator, with power reserve for a delayed switch off at bus fault, is integrated.

Table 1. ORDERING INFORMATION(1)(2)

T_A	PACKAGE		ORDERABLE PART NUMBER
0°C to 70°C	SOIC – D	Reel of 2500	TSS721ADR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DESCRIPTION

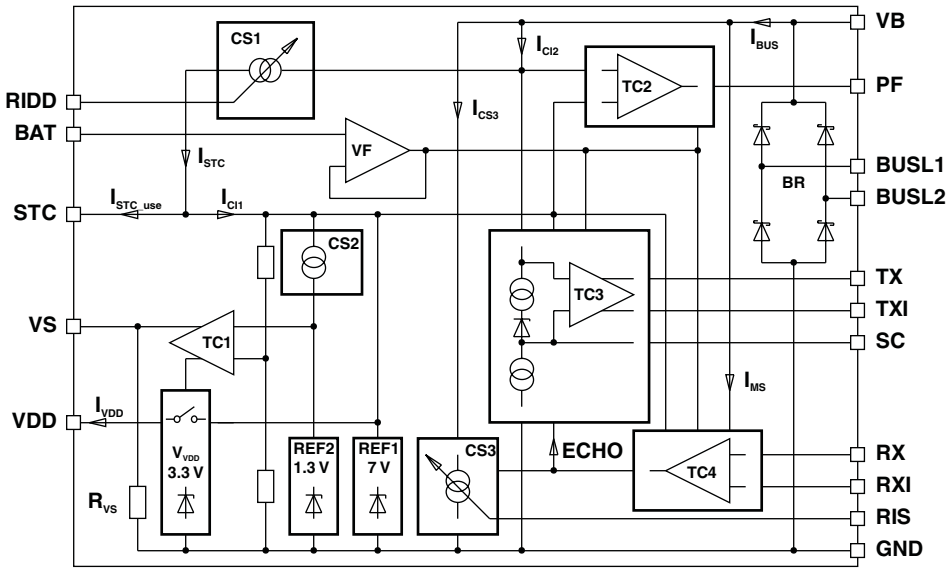


Figure 1. Functional Schematic

Table 2. Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
BUSL2	1	Meter-Bus
VB	2	Differential bus voltage after rectifier
STC	3	Support capacitor
RIDD	4	Current adjustment input
PF	5	Power fail output
SC	6	Sampling capacitor
TXI	7	Data output inverted
TX	8	Data output
BAT	9	Logic level adjust
VS	10	Switch for bus or battery supply output
VDD	11	Voltage regulator output
RX	12	Data input
RXI	13	Data input inverted
RIS	14	Adjust input for modulation current
GND	15	Ground
BUSL1	16	Meter-Bus

Data Transmission, Master to Slave

The mark level on the bus lines V_{BUS} = MARK is defined by the difference of BUSL1 and BUSL2 at the slave. It is dependent on the distance of Master to Slave, which affects the voltage drop on the wire. To make the receiver independent, a dynamic reference level on the SC pin is used for the voltage comparator TC3 (see Figure 2).

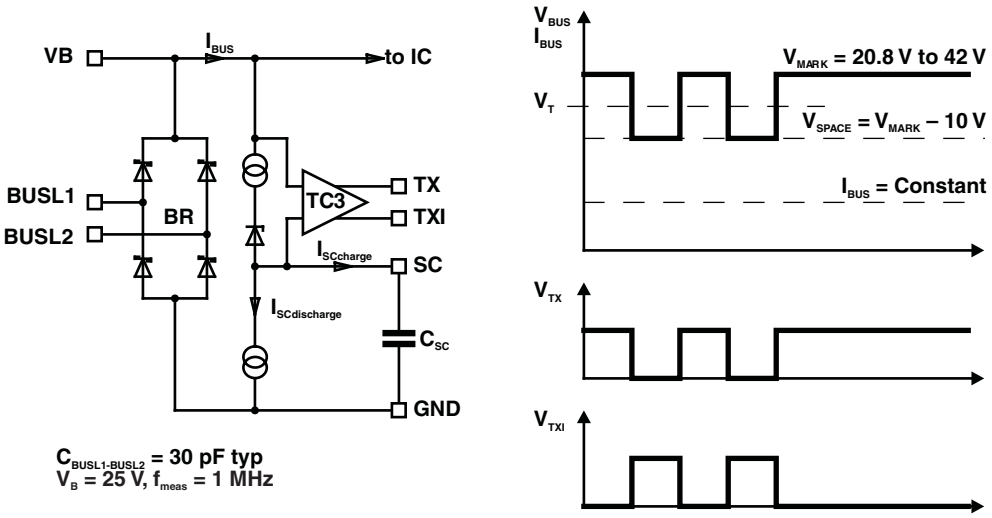


Figure 2. Data Transmission, Master to Slave

A capacitor C_{SC} at pin SC is charged by a current $I_{SCcharge}$ and is discharged with a current $I_{SCdischarge}$ where:

$$I_{SCdisharge} = \frac{I_{SCcharge}}{40\ (typ)} \quad (1)$$

This ratio is necessary to run any kind of UART protocol independent of the data contents. (for example, if an 11-bit UART protocol is transmitted with all data bits at 0 and only the stop bit at 1). There must be sufficient time to recharge the capacitor C_{SC}. The input level detector TC3 detects voltage modulations from the master, V_{BUS} = SPACE/MARK conditions, and switches the inverted output TXI and the non-inverted output TX.

Data Transmission, Slave to Master

The device uses current modulation to transmit information from the slave to the master while the bus voltage remains constant. The current source CS3 modulates the bus current and the master detects the modulation. The constant current source CS3 is controlled by the inverted input RXI or the non-inverted input RX. The current source CS3 can be programmed by an external resistor R_{RIS}. The modulation supply current I_{MS} flows in addition to the current source CS3 during the modulation time.

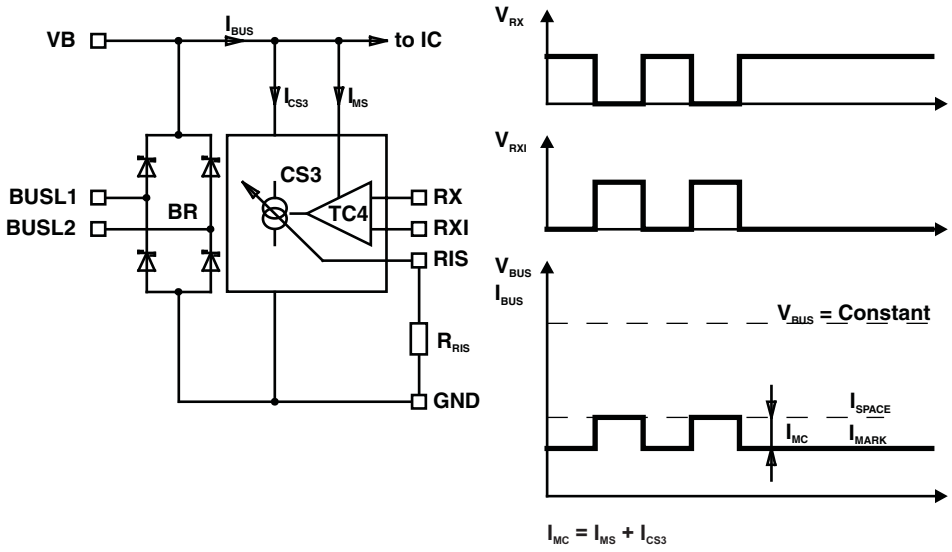
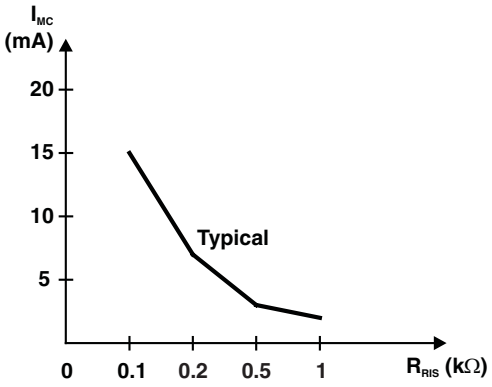


Figure 3. Data Transmission, Slave to Master

Because the TSS721A is configured for half-duplex only, the current modulation from RX or RXI is repeated concurrently as ECHO on the outputs TX and TXI. If the slave, as well as the master, is trying to send information via the lines, the added signals appear on the outputs TX and TXI, which indicates the data collision to the slave (see Figure 1).

The bus topology requires a constant current consumption by each connected slave.

To calculate the value of the programming resistor R_{RIS}, use the formula shown in Figure 4.



$$R_{RIS} = \frac{V_{RIS}}{I_{CS3}} = \frac{V_{RIS}}{I_{MC} - I_{MS}}$$

V_{RIS} = Voltage on pin RIS
R_{RIS} = Programming resistor
I_{CS3} = Programmable current
I_{MC} = Modulation current
I_{MS} = Modulation supply current (220 µA typ)

Figure 4. Calculate Programming Resistor R_{RIS}

Slave Supply, 3.3 V

The TSS721A has an internal 3.3-V voltage regulator. The output power of this voltage regulator is supplied by the storage capacitor C_{STC} at pin STC. The storage capacitor C_{STC} at pin STC is charged with constant current I_{STC_use} from the current source CS1. The maximum capacitor voltage is limited to REF1. The charge current I_{STC} has to be defined by an external resistor at pin RIDD.

The adjustment resistor R_{RIDD} can be calculated using Equation 2.

$$R_{RID} = 25 \frac{V_{RIDD}}{I_{STC}} = 25 \frac{V_{RIDD}}{I_{STC\_use} + I_{IC1}} \quad (2)$$

Where,

I_{STC} = current from current source CS1
I_{STC_use} = charge current for support capacitor
I_{CI} = internal current
V_{RIDD} = voltage on pin RIDD
R_{RIDD} = value of adjustment resistor

The voltage level of the storage capacitor C_{STC} is monitored with comparator TC1. Once the voltage V_{STC} reaches V_{VDD_on}, the switch S_{VDD} connects the stabilized voltage V_{VDD} to pin VDD. VDD is turned off if the voltage V_{STC} drops below the V_{VDD_off} level.

Voltage variations on the capacitor C_{STC} create bus current changes (see Figure 5).

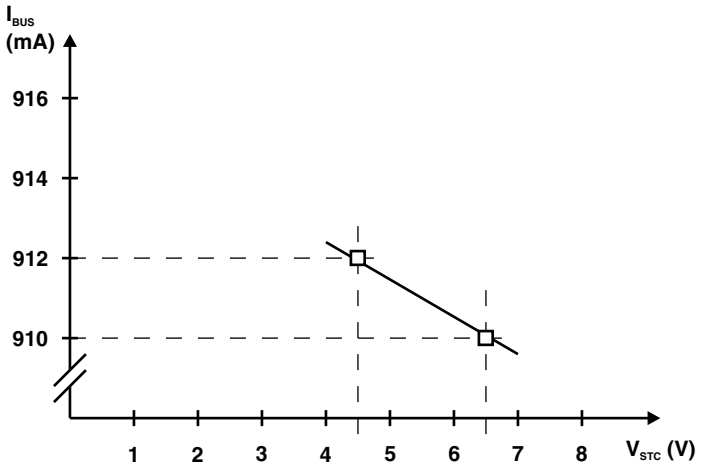


Figure 5. Single Mode Bus Load

At a bus fault the shut down time of VDD (t_{off}) in which data storage can be performed depends on the system current I_{VDD} and the value of capacitor C_{STC}. See Figure 6, which shows a correlation between the shutdown of the bus voltage V_{BUS} and V_{DD_off} and t_{off} for dimensioning the capacitor.

The output VS is meant for slave systems that are driven by the bus energy, as well as from a battery should the bus line voltage fail. The switching of VS is synchronized with VDD and is controlled by the comparator TC1. An external transistor at the output VS allows switching from the Meter-Bus remote supply to battery.

Power On/Off

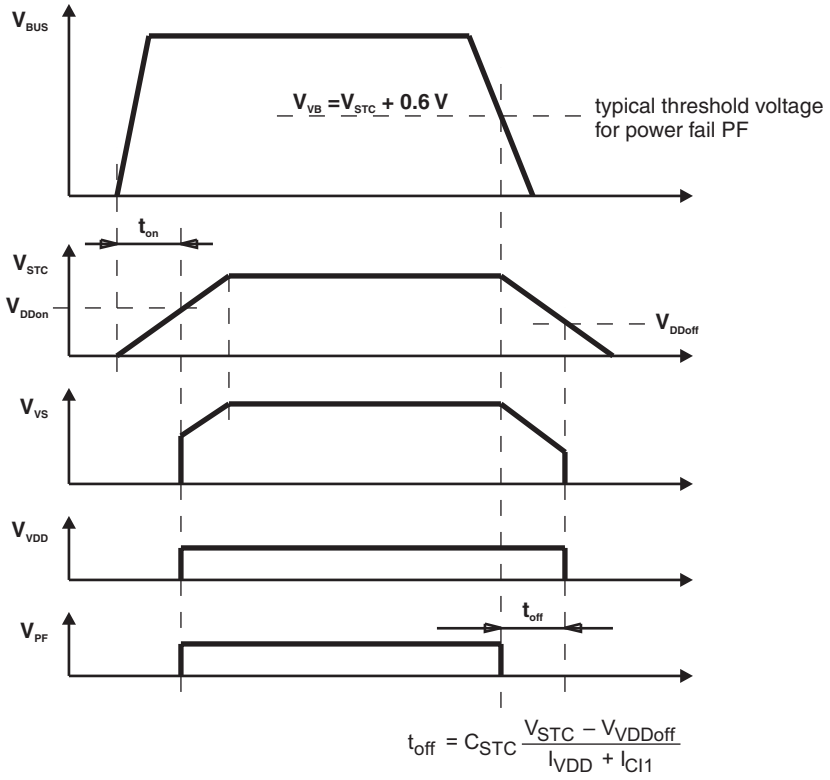


Figure 6. Power On/Off Timing

Power Fail Function

Because of the rectifier bridge BR at the input, BUSL1, and BUSL2, the TSS721A is polarity independent. The pin VB to ground (GND) delivers the bus voltage V_{VB} less the voltage drop over the rectifier BR. The voltage comparator TC2 monitors the bus voltage. If the voltage $V_{VB} > V_{STC} + 0.6$ V, then the output PF = 1. The output level PF = 0 (power fail) provides a warning of a critical voltage drop to the microcontroller to save the data immediately.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

V_{MB}	Voltage, BUSL1 to BUSL2		±50 V
V_I	Input voltage range	RX and RXI	–0.3 V to 5.5 V
		BAT	–0.3 V to 5.5 V
T_J	Operating junction temperature range		–25°C to 150°C
T_A	Operating free-air temperature range		–25°C to 85°C
T_{STG}	Storage temperature range		–65°C to 150°C
	Power derating factor, junction to ambient		8 mW/°C

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{MB}	Bus voltage, |BUSL2 – BUSL1|	Receiver	10.8	42	V
		Transmitter	12	42	
V_I	Input voltage	VB (receive mode)	9.3		V
		BAT(2)	2.5	3.8	
R_{RIDD}	RIDD resistor		13	80	kΩ
R_{RIS}	RIS resistor		100		Ω
T_A	Operating free-air temperature		–25	85	°C

(1) All voltage values are measured with respect to the GND terminal unless otherwise noted.
(2) $V_{BAT}(max) \le V_{STC} - 1$ V

ELECTRICAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{BR}	Voltage drop at rectifier BR	I_{BUS} = 3 mA				1.5	V
ΔV_{CS1}	Voltage drop at current source CS1	R_{RIDD} = 13 kΩ				1.8	V
I_{BUS}	BUS current	V_{STC} = 6.5 V, I_{MC} = 0 mA	R_{RIDD} = 13 kΩ			3	mA
			R_{RIDD} = 30 kΩ			1.5	
ΔI_{BUS}	BUS current accuracy	ΔV_{BUS} = 10 V, I_{MC} = 0 mA, R_{RIDD} = 13 kΩ to 30 kΩ				2	%
I_{CC}	Supply current	V_{STC} = 6.5 V, I_{MC} = 0 mA, V_{BAT} = 3.8 V, R_{RIDD} = 13 kΩ(2)				650	µA
I_{CI1}	CI1 current	V_{STC} = 6.5 V, I_{MC} = 0 mA, V_{BAT} = 3.8 V, R_{RIDD} = 13 kΩ, V_{BUS} = 6.5 V, RX/RXI = off (2)				350	µA
I_{BAT}	BAT current			–0.5		0.5	µA
$I_{BAT} + I_{VDD}$	BAT plus VDD current	V_{BUS} = 0 V, V_{STC} = 0 V		–0.5		0.5	µA
V_{VDD}	VDD voltage	$-I_{VDD}$ = 1 mA, V_{STC} = 6.5 V		3.1		3.4	V
R_{VDD}	VDD resistance	$-I_{VDD}$ = 2 to 8 mA, V_{STC} = 4.5 V				5	Ω
V_{STC}	STC voltage	V_{DD} = on, VS = on		5.6		6.4	V
		V_{DD} = off, VS = off		3.8		4.3	
		$I_{VDD} < I_{STC\_use}$		6.5		7.5	
I_{STC_use}	STC current	V_{STC} = 5 V	R_{RIDD} = 30 kΩ	0.65		1.1	mA
			R_{RIDD} = 13 kΩ	1.85		2.4	
V_{RIDD}	RIDD voltage	R_{RIDD} = 30 kΩ		1.23		1.33	V
V_{VS}	VS voltage	V_{DD} = on, I_{VS} = –5 µA		V_{STC} – 0.4		V_{STC}	V
R_{VS}	VS resistance	V_{DD} = off		0.3		1	MΩ
V_{PF}	PF voltage	V_{STC} = 6.5 V	$V_{VB} = V_{STC} + 0.8$ V, I_{PF} = –100 µA	V_{BAT} – 0.6		V_{BAT}	V
			$V_{VB} = V_{STC} + 0.3$ V, I_{PF} = 1 µA	0		0.6	
			$V_{VB} = V_{STC} + 0.3$ V, I_{PF} = 5 µA	0		0.9	

(1) All voltage values are measured with respect to the GND terminal, unless otherwise noted.
(2) Inputs RX/RXI and outputs TX/TXI are open, $I_{CC} = I_{CI1} + I_{CI2}$

ELECTRICAL CHARACTERISTICS(1) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	C_{STC} = 50 µF, Bus voltage slew rate: 1 V/µs			3	s

RECEIVER SECTION ELECTRICAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T		See Figure 2	MARK – 8.2		MARK – 5.7	V
V_{SC}	SC voltage				V_{VB}	V
$I_{SCcharge}$	SC charge current	V_{SC} = 24 V, V_{VB} = 36 V	–15		–40	µA
$I_{SCdischarge}$	SC discharge current	V_{SC} = V_{VB} = 24 V	0.3		–0.033 × $I_{SCcharge}$	µA
V_{OH}	High-level output voltage (TX, TXI)	I_{TX}/I_{TXI} = –100 µA (see Figure 2)	V_{BAT} – 0.6		V_{BAT}	V
V_{OL}	Low-level output voltage (TX, TXI)	I_{TX}/I_{TXI} = 100 µA	0		0.5	V
		I_{TX} = 1.1 mA	0		1.5	
I_{TX} I_{TXI}	TX, TXI current	V_{TX} = 7.5, V_{VB} = 12 V, V_{STC} = 6 V, V_{BAT} = 3.8 V			10	µA

(1) All voltage values are measured with respect to the GND terminal, unless otherwise noted.

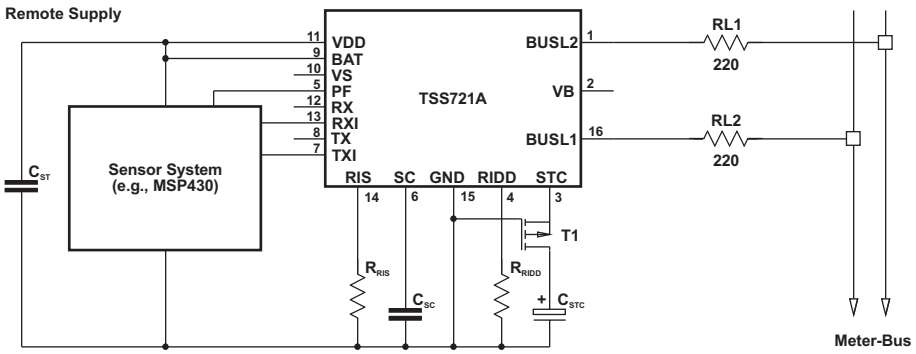
TRANSMITTER SECTION ELECTRICAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MC}	MC voltage	R_{RIS} = 100 Ω	11.5		19.5	mA
V_{RIS}	RIS voltage	R_{RIS} = 100 Ω	1.4		1.7	V
		R_{RIS} = 1000 Ω	1.5		1.8	
V_{IH}	High-level input voltage (RX, RXI)	See Figure 3, see (2)	V_{BAT} – 0.8		5.5	V
V_{IL}	Low-level input voltage (RX, RXI)	See Figure 3	0		0.8	V
I_{RX}	RX current	V_{RX} = V_{BAT} = 3 V, V_{VB} = V_{STC} = 0 V	-0.5		0.5	µA
		V_{RX} = 0 V, V_{BAT} = 3 V, V_{STC} = 6.5 V	-10		-40	
I_{RXI}	RXI current	V_{RXI} = V_{BAT} = 3 V, V_{VB} = V_{STC} = 0 V	10		40	µA
		V_{RXI} = V_{BAT} = 3 V, V_{STC} = 6.5 V	10		40	

(1) All voltage values are measured with respect to the GND terminal, unless otherwise noted.
(2) V_{IH}(max) = 5.5 V is valid only when V_{STC} > = 6.5 V.

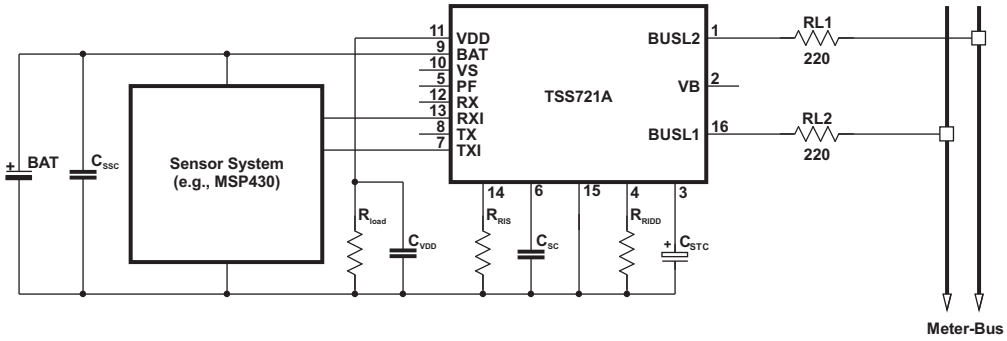
APPLICATION INFORMATION



R_{RIDD} = 30 kΩ	C_{STC} =< 220 µF	single load 1UL
R_{RIDD} = 13 kΩ	C_{STC} =< 470 µF	double load 2UL

NOTE: Transistor T1 should be a BSS84.

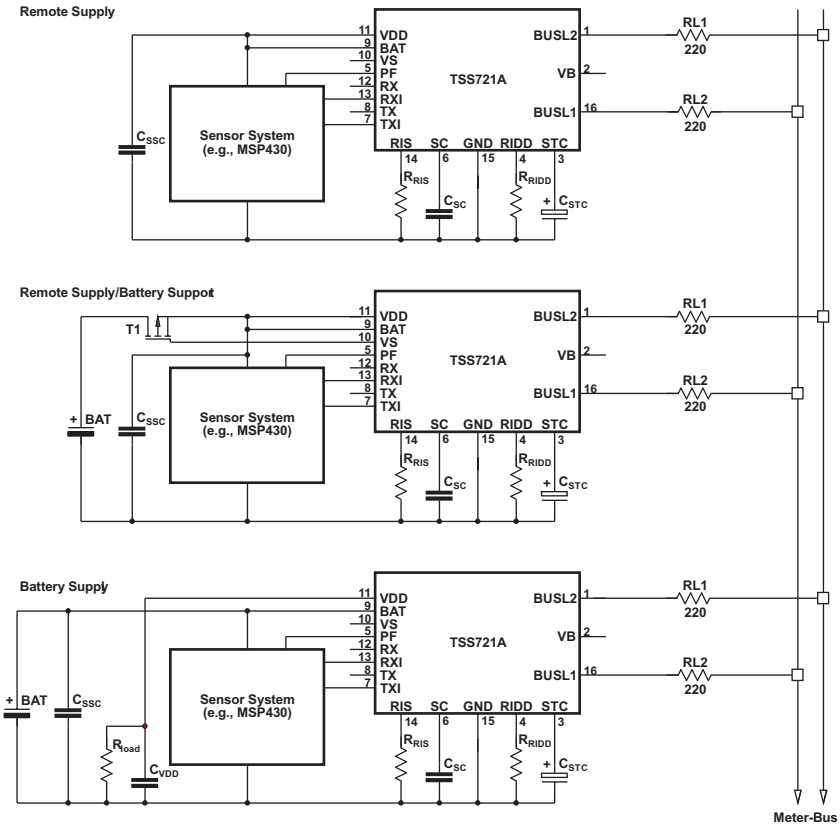
Figure 7. Basic Application Circuit Using Support Capacitor C_{STC} > 50 µF



C_{SSC} - system stabilising capacitor
C_{STC} - support capacitor
C_{SC} - sampling capacitor
C_{VDD} - stabilising capacitor (100 nF)
C_{STC}:C_{VDD} >= 4:1

R_{RIDD} - slave-current adjustment resistor
R_{RIS} - modulation-current resistor
RL1,RL2 - protection resistors
R_{load} - discharge resistor (100 kΩ recommended)

Figure 8. Basic Application Circuit for Supply From Battery



NOTE: R_{DSon} of the transistor T1 (BSS84) at low battery voltage must be considered during application design.

Figure 9. Basic Applications for Different Supply Modes

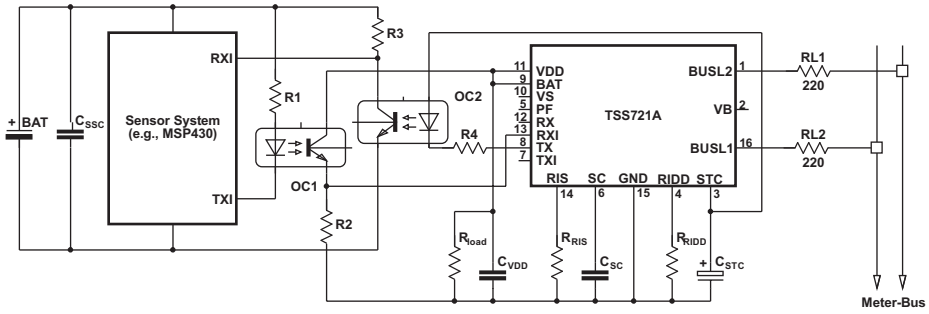


Figure 10. Basic Optocoupler Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TSS721AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TSS721ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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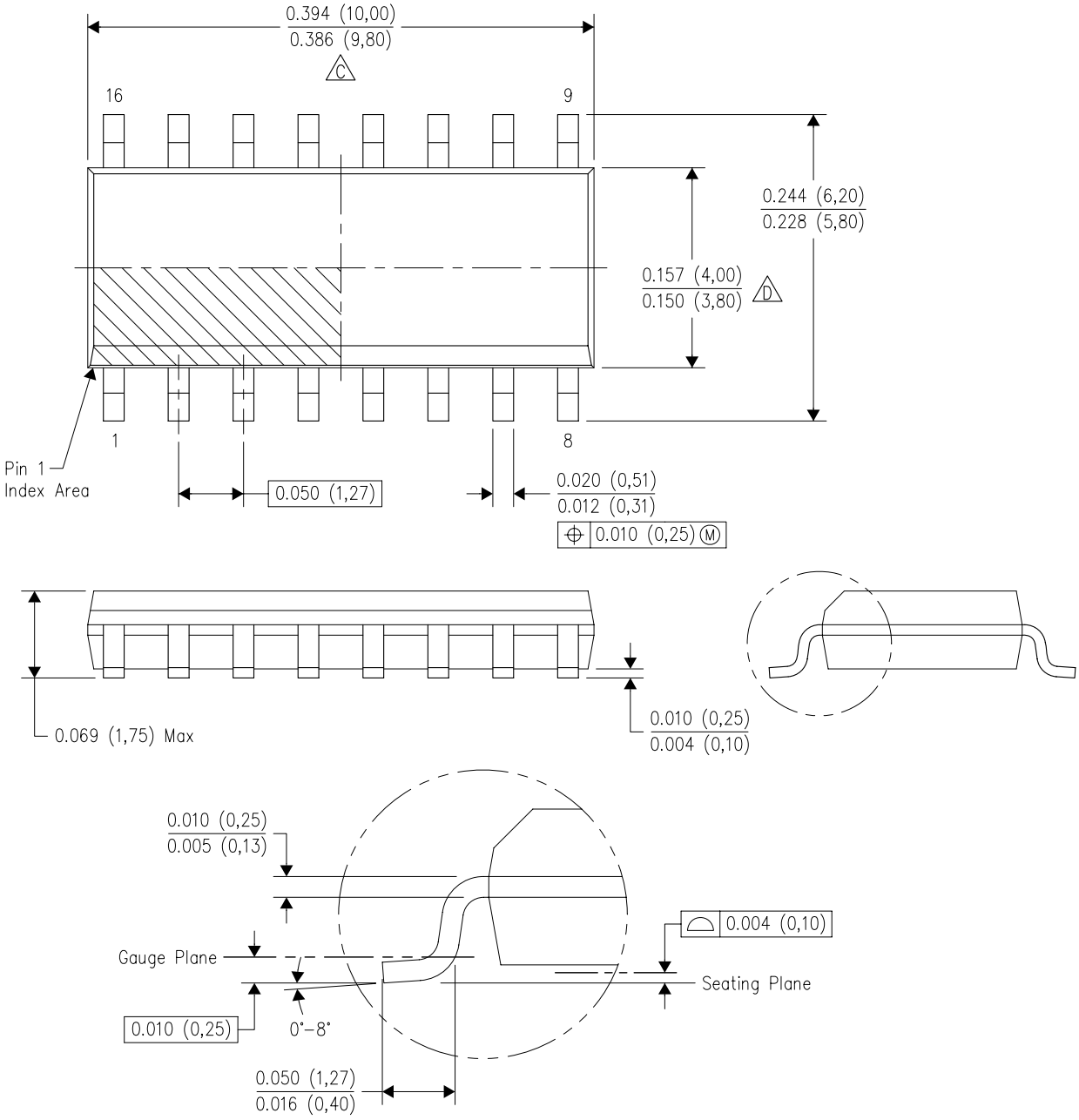
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

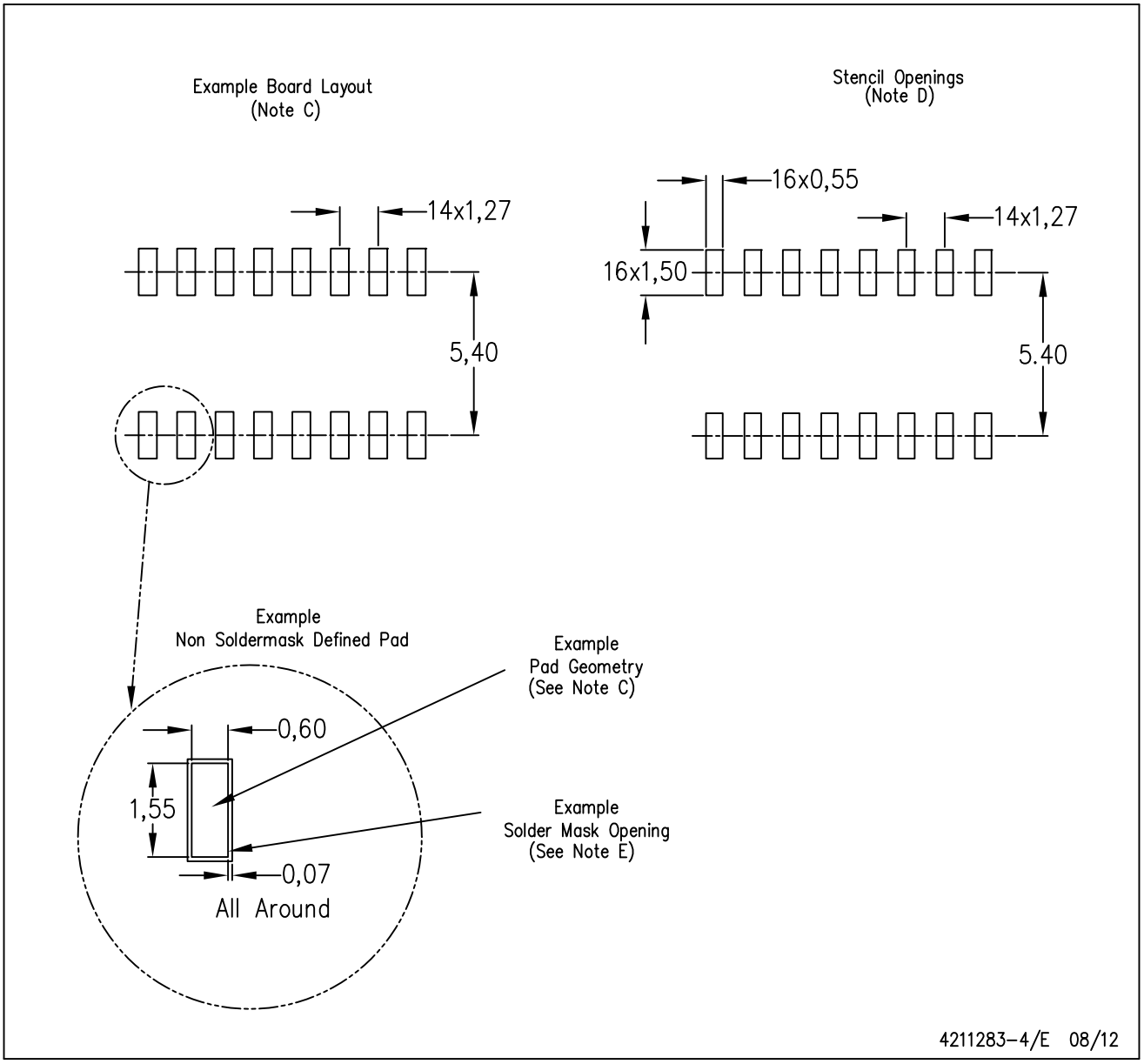
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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