N-Channel Controller for Constant Current LED Drivers

Check for Samples: LM3429, LM3429-Q1

FEATURES

- **LM3429Q1 is an Automotive Grade Product That is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)**
- **V_{IN} Range From 4.5V to 75V**
- **Adjustable Current Sense Voltage**
- **High-Side Current Sensing**
- **2Ω, 1A Peak MosFET Gate Driver**
- **Input Under-Voltage Protection**
- **Over-Voltage Protection**
- **PWM Dimming**
- **Analog Dimming**
- **Cycle-by-Cycle Current Limit**
- **Programmable Switching Frequency**
- **Thermal Shutdown**

APPLICATIONS

- **LED Drivers - Buck, Boost, Buck-Boost, SEPIC**
- **Indoor and Outdoor SSL**
- **Automotive**
- **General Illumination**
- **Constant-Current Regulators**

DESCRIPTION

The LM3429 is a versatile high voltage N-channel MosFET controller for LED drivers . It can be easily configured in buck, boost, buck-boost and SEPIC topologies. This flexibility, along with an input voltage rating of 75V, makes the LM3429 ideal for illuminating LEDs in a very diverse, large family of applications.

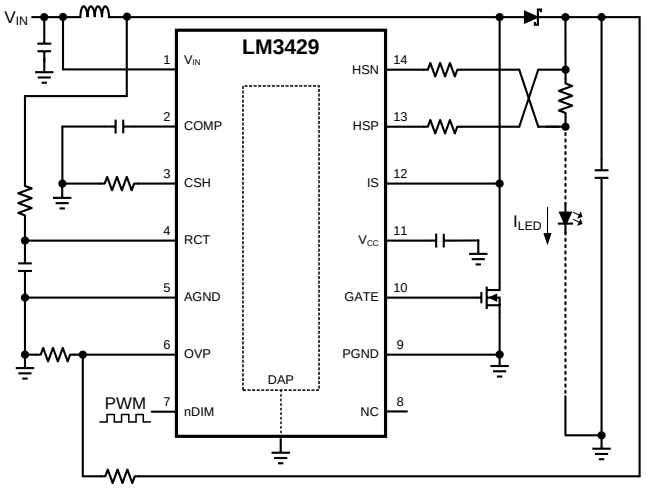
Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3429 uses Predictive Off-time (PRO) control, which is a combination of peak current-mode control and a predictive off-timer. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

The LM3429 includes a high-voltage startup regulator that operates over a wide input range of 4.5V to 75V. The internal PWM controller is designed for adjustable switching frequencies of up to 2.0 MHz, thus enabling compact solutions. Additional features include analog dimming, PWM dimming, over-voltage protection, under-voltage lock-out, cycle-by-cycle current limit, and thermal shutdown.

The LM3429 comes in a low profile, thermally efficient TSSOP 14-lead package.

The LM3429Q1 is an Automotive Grade product that is AEC-Q100 grade 1 qualified

Typical Boost Application Circuit



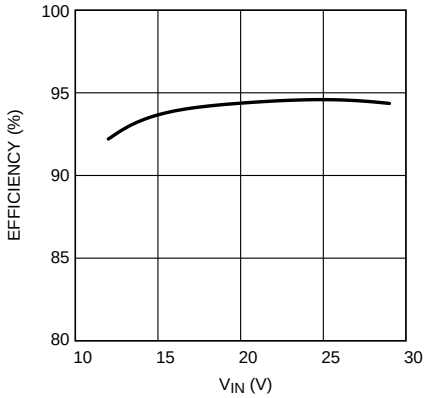


Figure 1. Boost Evaluation Board 9 Series LEDs at 1A

Connection Diagram

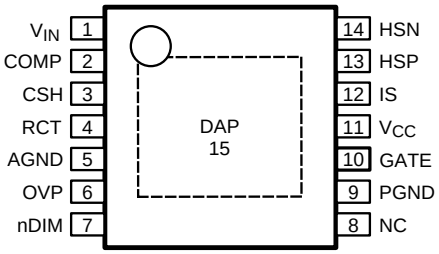


Figure 2. 14-Lead TSSOP

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	V_{IN}	Input Voltage	Bypass with 100 nF capacitor to AGND as close to the device as possible in the circuit board layout.
2	COMP	Compensation	Connect a capacitor to AGND to set compensation.
3	CSH	Current Sense High	Connect a resistor to AGND to set signal current. For analog dimming, connect current source or potentiometer to AGND (see ANALOG DIMMING section).
4	RCT	Resistor Capacitor Timing	Connect a resistor from the switch node and a capacitor to AGND to set the switching frequency.
5	AGND	Analog Ground	Connect to PGND through the DAP copper circuit board pad to provide proper ground return for CSH, COMP, and RCT.
6	OVP	Over-Voltage Protection	Connect to a resistor divider from V_O to program output over-voltage lockout (OVLO). Turn-off threshold is 1.24V and hysteresis for turn-on is provided by 20 µA current source.
7	nDIM	Not DIM input	Connect a PWM signal for dimming as detailed in the PWM DIMMING section and/or a resistor divider from V_{IN} to program input under-voltage lockout (UVLO). Turn-on threshold is 1.24V and hysteresis for turn-off is provided by 20 µA current source.
8	NC	No Connection	Leave open.
9	PGND	Power Ground	Connect to AGND through DAP copper pad to provide ground return for GATE.
10	GATE	Gate Drive Output	Connect to the gate of the external NFET.
11	V_{CC}	Internal Regulator Output	Bypass with a 2.2 µF–3.3 µF, ceramic capacitor to PGND.
12	IS	Main Switch Current Sense	Connect to the drain of the main N-channel MosFET switch for R_{DS-ON} sensing or to a sense resistor installed in the source of the same device.
13	HSP	LED Current Sense Positive	Connect through a series resistor to LED current sense resistor (positive).
14	HSN	LED Current Sense Negative	Connect through a series resistor to LED current sense resistor (negative).
DAP (15)	DAP	Thermal pad on bottom of IC	Connect to AGND and PGND. For thermal considerations see (1).

(1) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for a reference layout wherein the 14L TSSOP package has its DAP pad populated with 9 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be 104 °C/W for the 14L TSSOP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{IN}, nDIM	-0.3V to 76.0V -1 mA continuous
OVP, HSP, HSN	-0.3V to 76.0V -100 µA continuous
RCT	-0.3V to 3.0V -1 mA to +5 mA continuous
IS	-0.3V to 76.0V -2V for 100 ns -1 mA continuous
V_{CC}	-0.3V to 8.0V
COMP, CSH	-0.3V to 6.0V -200 µA to +200 µA Continuous
GATE	-0.3V to V_{CC} -2.5V for 100 ns V_{CC}+2.5V for 100 ns -1 mA to +1 mA continuous
PGND	-0.3V to 0.3V -2.5V to 2.5V for 100 ns
Maximum Junction Temperature	Internally Limited
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Reflow and Solder) (3)	260°C
Continuous Power Dissipation	Internally Limited
ESD Susceptibility (4), Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Refer to http://www.ti.com/packaging for more detailed information and mounting techniques.
(4) Human Body Model, applicable std. JESD22-A114-C.

Operating Conditions (1)

Operating Junction Temperature Range	−40°C to +125°C
Input Voltage V_{IN}	4.5V to 75V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.

Electrical Characteristics (1)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
STARTUP REGULATOR (V_{CC})						
V_{CC-REG}	V_{CC} Regulation	I_{CC} = 0 mA	**6.30**	6.90	**7.35**	V
I_{CC-LIM}	V_{CC} Current Limit	V_{CC} = 0V	**20**	27		mA
I_Q	Quiescent Current	Static		1.6	**3.0**	mA
$V_{CC-UVLO}$	V_{CC} UVLO Threshold	V_{CC} Increasing		4.17	**4.50**	V
		V_{CC} Decreasing	**3.70**	4.08		V
V_{CC-HYS}	V_{CC} UVLO Hysteresis			0.1		V
OVER-VOLTAGE PROTECTION (OVP)						
V_{TH-OVP}	OVP OVLO Threshold	OVP Increasing	**1.180**	1.240	**1.280**	V
$I_{HYS-OVP}$	OVP Hysteresis Source Current	OVP Active (high)	**10**	20	**30**	µA
ERROR AMPLIFIER						
V_{CSH}	CSH Reference Voltage	With Respect to AGND	**1.210**	1.235	**1.260**	V
	Error Amplifier Input Bias Current		-0.6	0	0.6	µA
	COMP Sink / Source Current		**10**	26	**40**	µA
	Transconductance			100		µA/V
	Linear Input Range	(4)		±125		mV
	Transconductance Bandwidth	-6dB Unloaded Response(4)	0.5	1.0		MHz
OFF TIMER (RCT)						
$t_{OFF-MIN}$	Minimum Off-time	RCT = 1V through 1 kΩ		35	**75**	ns
R_{RCT}	RCT Reset Pull-down Resistance			36	**120**	Ω
V_{RCT}	V_{IN}/25 Reference Voltage	V_{IN} = 14V	**540**	565	**585**	mV
PWM COMPARATOR						
	COMP to PWM Offset		**700**	800	**900**	mV
CURRENT LIMIT (IS)						
V_{LIM}	Current Limit Threshold		**215**	245	**275**	mV
	V_{LIM} Delay to Output			35	**75**	ns
t_{ON-MIN}	Leading Edge Blanking Time		**75**	250	**450**	ns
HIGH SIDE TRANSCONDUCTANCE AMPLIFIER						
	Input Bias Current			10		µA
	Transconductance		**20**	119		mA/V
	Input Offset Current		**-1.5**	0	**1.5**	µA
	Input Offset Voltage		**-7**	0	**7**	mV
	Transconductance Bandwidth	I_{CSH} = 100 µA(4)	250	500		kHz
GATE DRIVER (GATE)						
$R_{SRC(GATE)}$	GATE Sourcing Resistance	GATE = High		2.0	**6.0**	Ω
$R_{SNK(GATE)}$	GATE Sinking Resistance	GATE = Low		1.3	**4.5**	Ω

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.

(2) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(3) Typical numbers are at 25°C and represent the most likely norm.

(4) These electrical parameters are specified by design, and are not verified by test.

Electrical Characteristics [1] (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
UNDER-VOLTAGE LOCKOUT and DIM INPUT (nDIM)						
$V_{TH-nDIM}$	nDIM / UVLO Threshold		**1.180**	1.240	**1.280**	V
$I_{HYS-nDIM}$	nDIM Hysteresis Current		**10**	20	**30**	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold	[4]		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	[4]		25		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient[5]	14L TSSOP		40		°C/W
θ_{JC}	Junction to Exposed Pad (DAP)	14L TSSOP		5.5		°C/W

(5) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for a reference layout wherein the 14L TSSOP package has its DAP pad populated with 9 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be 104 °C/W for the 14L TSSOP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

Typical Performance Characteristics

T_A=+25°C and V_{IN} = 14V unless otherwise specified

Boost Efficiency vs. Input Voltage
V_O = 32V (9 LEDs)(1)

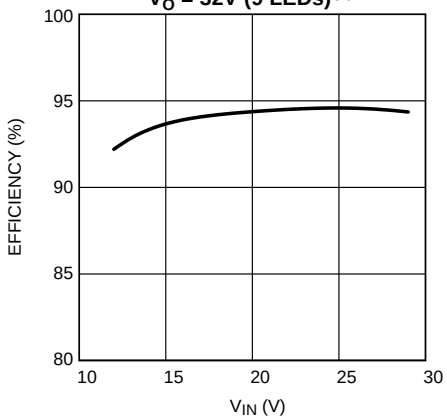


Figure 3.

Buck-Boost Efficiency vs. Input Voltage
V_O = 20V (6 LEDs)(2)

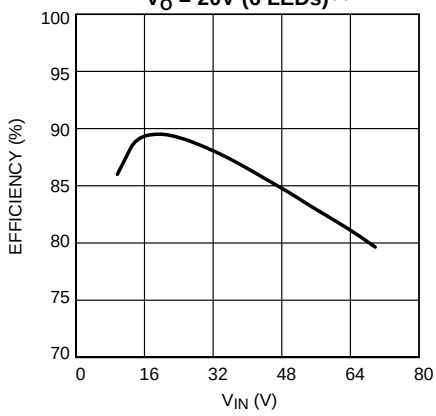


Figure 4.

Boost LED Current vs. Input Voltage
V_O = 32V (9 LEDs)(1)

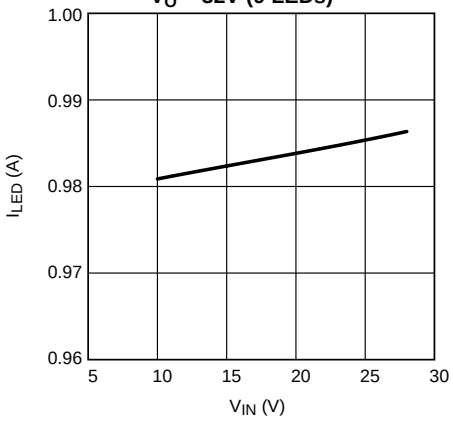


Figure 5.

Buck-boost LED Current vs. Input Voltage
V_O = 20V (6 LEDs)(2)

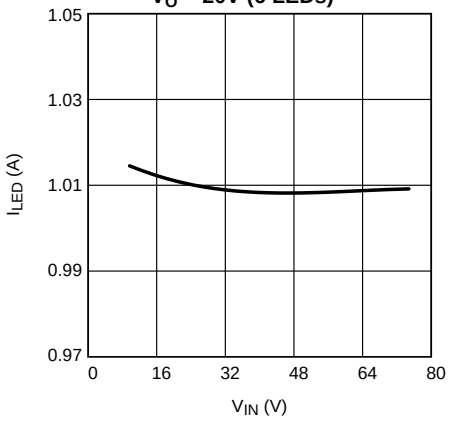


Figure 6.

Analog Dimming
V_O = 20V (6 LEDs)(2)

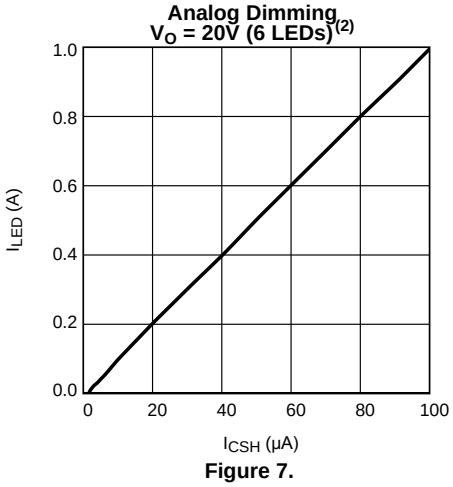


Figure 7.

PWM Dimming
V_O = 20V (6 LEDs)(2)

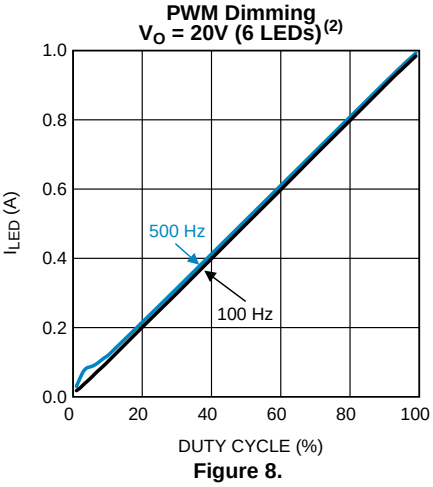


Figure 8.

(1) The measurements were made using the standard boost evaluation board from AN-1986 (SNVA404).
(2) The measurements were made using the standard buck-boost evaluation board from AN-1985 (SNVA403).

Typical Performance Characteristics (continued)

T_A=+25°C and V_{IN} = 14V unless otherwise specified

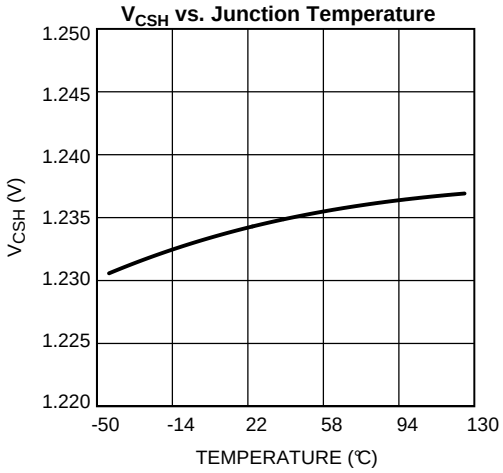


Figure 9.

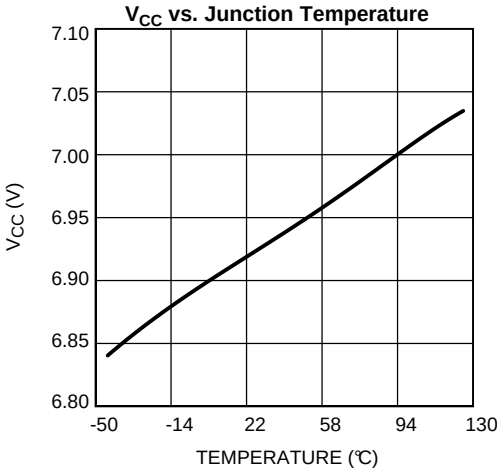


Figure 10.

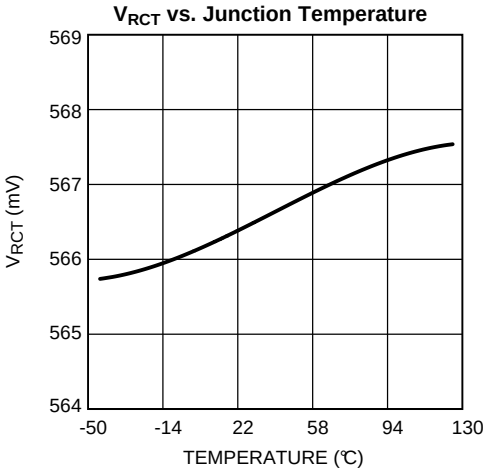


Figure 11.

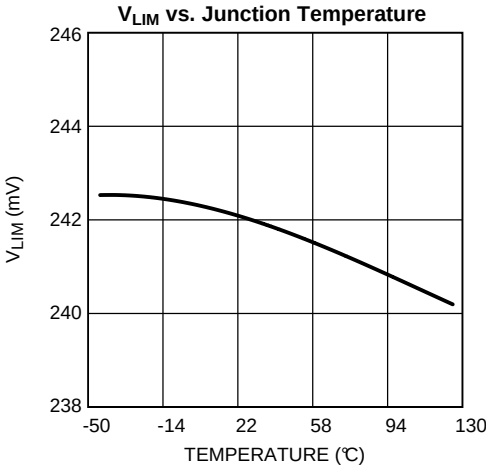


Figure 12.

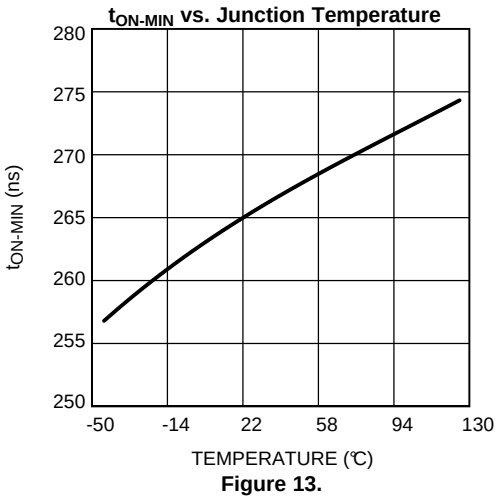
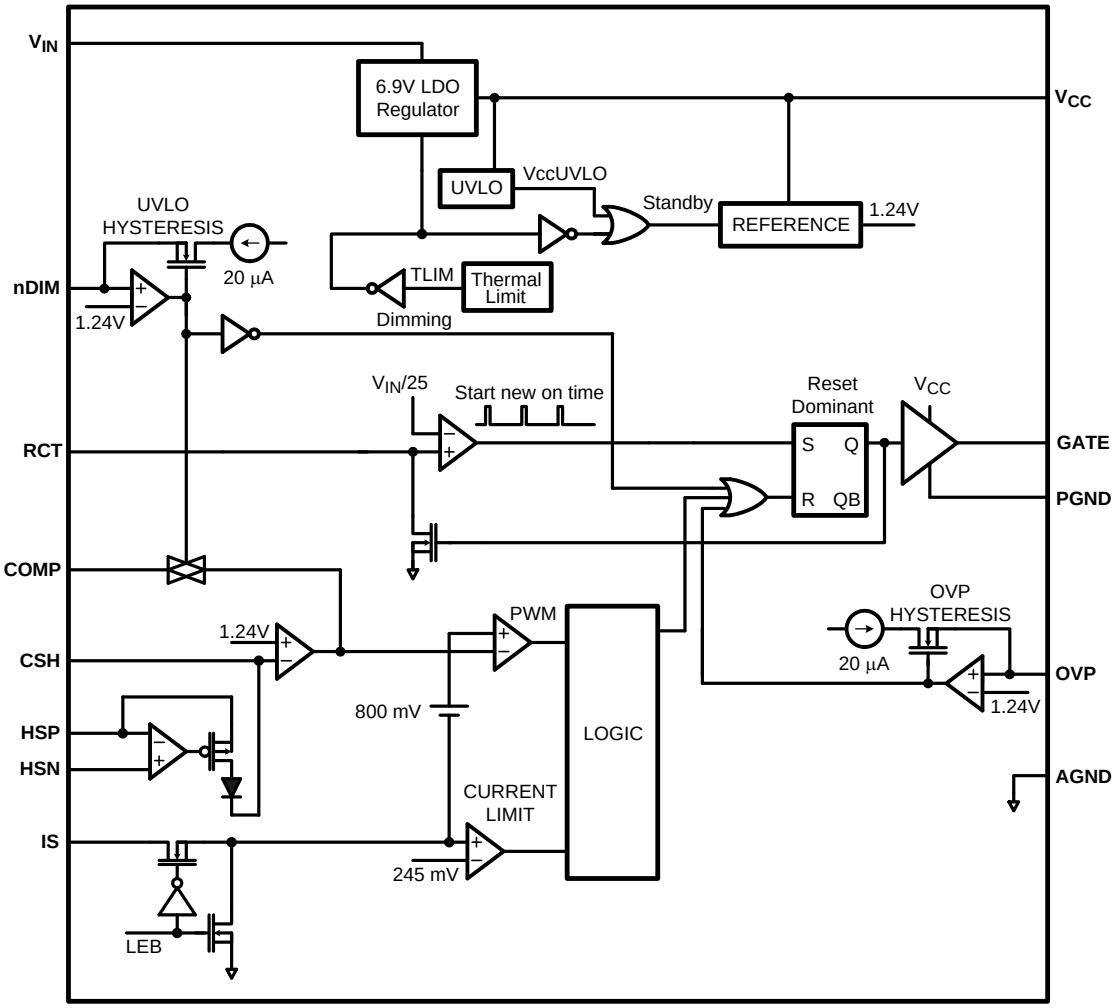


Figure 13.

BLOCK DIAGRAM



Theory of Operation

The LM3429 is an N-channel MosFET (NFET) controller for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM3429 uses a Predictive Off-time (PRO) control architecture that allows the regulator to be operated using minimal external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the output enable/disable function allows for PWM dimming using no external components. When designing, the maximum attainable LED current is not internally limited because the LM3429 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3429 to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

CURRENT REGULATORS

Current regulators can be designed to accomplish three basic functions: buck, boost, and buck-boost. All three topologies in their most basic form contain a main switching MosFET, a recirculating diode, an inductor and capacitors. The LM3429 is designed to drive a ground referenced NFET which is perfect for a standard boost regulator. Buck and buck-boost regulators, on the other hand, usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch can be used to drive a floating load instead. The LM3429 can then be used to drive all three basic topologies as shown in the Basic Topology Schematics section.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 14 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

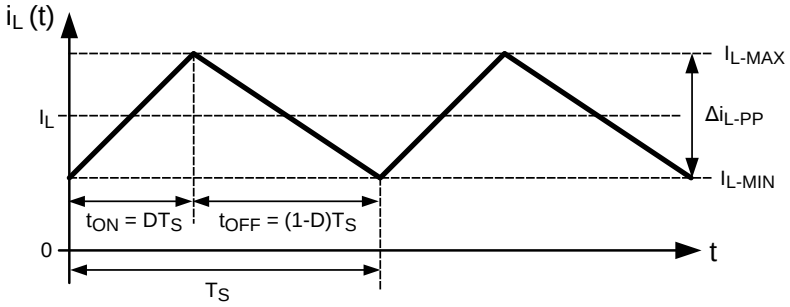


Figure 14. Ideal CCM Regulator Inductor Current $i_L(t)$

The average output LED current (I_{LED}) is proportional to the average inductor current (I_L) , therefore if I_L is tightly controlled, I_{LED} will be well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

Buck

$$D = \frac{V_O}{V_{IN}} \quad (1)$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (2)$$

Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \quad (3)$$

PREDICTIVE OFF-TIME (PRO) CONTROL

PRO control is used by the LM3429 to control I_{LED}. It is a combination of average peak current control and a one-shot off-timer that varies with input voltage. The LM3429 uses peak current control to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MosFET path or the MosFET R_{DS-ON} for both cycle-by-cycle current limit and input voltage feed forward. D is indirectly controlled by changes in both t_{OFF} and t_{ON}, which vary depending on the operating point.

Even though the off-time control is quasi-hysteretic, the input voltage proportionality in the off-timer creates an essentially constant switching frequency over the entire operating range for boost and buck-boost topologies. The buck topology can be designed to give constant ripple over either input voltage or output voltage, however switching frequency is only constant at a specific operating point .

This type of control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. The averaging mechanism in the peak detection control loop provides extremely accurate LED current regulation over the entire operating range.

PRO control was designed to mitigate “current mode instability” (also called “sub-harmonic oscillation”) found in standard peak current mode control when operating near or above 50% duty cycles. When using standard peak current mode control with a fixed switching frequency, this condition is present, regardless of the topology. However, using a constant off-time approach, current mode instability cannot occur, enabling easier design and control.

Predictive off-time advantages:

- There is no current mode instability at any duty cycle.
- Higher duty cycles / voltage transformation ratios are possible, especially in the boost regulator.

The only disadvantage is that synchronization to an external reference frequency is generally not available.

SWITCHING FREQUENCY

An external resistor (R_T) connected between the RCT pin and the switch node (where D1, Q1, and L1 connect), in combination with a capacitor (C_T) between the RCT and AGND pins, sets the off-time (t_{OFF}) as shown in Figure 15. For boost and buck-boost topologies, the V_{IN} proportionality ensures a virtually constant switching frequency (f_{SW}).

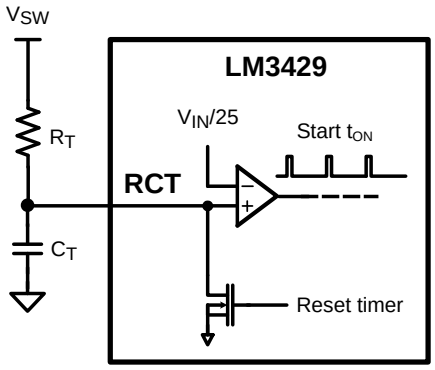


Figure 15. Off-timer Circuitry for Boost and Buck-boost Regulators

For a buck topology, R_T and C_T are also used to set t_{OFF}, however the V_{IN} proportionality will not ensure a constant switching frequency. Instead, constant ripple operation can be achieved. Changing the connection of R_T in Figure 15 from V_{SW} to V_{IN} will provide a constant ripple over varying V_{IN}. Adding a PNP transistor as shown in Figure 16 will provide constant ripple over varying V_O.

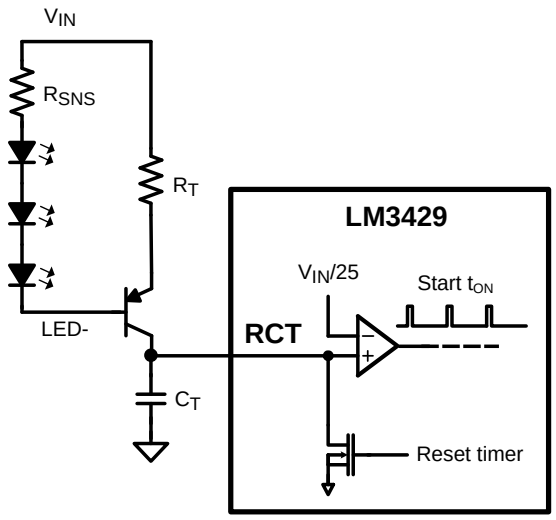


Figure 16. Off-timer Circuitry for Buck Regulators

The switching frequency is defined:

Buck (Constant Ripple vs. V_{IN})

$$f_{SW} = \frac{25 \times \left(V_{IN} - V_O\right)}{R_T \times C_T \times V_{IN}} \quad (4)$$

Buck (Constant Ripple vs. V_O)

$$f_{SW} = \frac{25 \times \left(V_{IN} \times V_O - V_O^2\right)}{R_T \times C_T \times V_{IN}^2} \quad (5)$$

Boost and Buck-boost

$$f_{SW} = \frac{25}{R_T \times C_T} \quad (6)$$

For all topologies, the C_T capacitor is recommended to be 1 nF and should be located very close to the LM3429.

AVERAGE LED CURRENT

The LM3429 uses an external current sense resistor (R_{SNS}) placed in series with the LED load to convert the LED current (I_{LED}) into a voltage (V_{SNS}) as shown in Figure 17. The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential (V_{HSP}=V_{HSN}) through negative feedback. Because of this, the V_{SNS} voltage is forced across R_{HSP} to generate the signal current (I_{CSH}) which flows out of the CSH pin and through the R_{CSH} resistor. The error amplifier will regulate the CSH pin to 1.24V, therefore I_{CSH} can be calculated:

$$I_{CSH} = \frac{V_{SNS}}{R_{HSP}} \quad (7)$$

This means V_{SNS} will be regulated as follows:

$$V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}} \quad (8)$$

I_{LED} can then be calculated:

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \quad (9)$$

The selection of the three resistors (R_{SNS}, R_{CSH}, and R_{HSP}) is not arbitrary. For matching and noise performance, the suggested signal current I_{CSH} is approximately 100 µA. This current does not flow in the LEDs and will not affect either the off state LED current or the regulated LED current. I_{CSH} can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum V_{SNS} is suggested to be 50 mV. Finally, a resistor (R_{HSN} = R_{HSP}) should be placed in series with the HSN pin to cancel out the effects of the input bias current (~10 µA) of both inputs of the high-side sense amplifier. Note that he CSH pin can also be used as a low-side current sense input regulated to the 1.24V. The high-side sense amplifier is disabled if HSP and HSN are tied to GND.

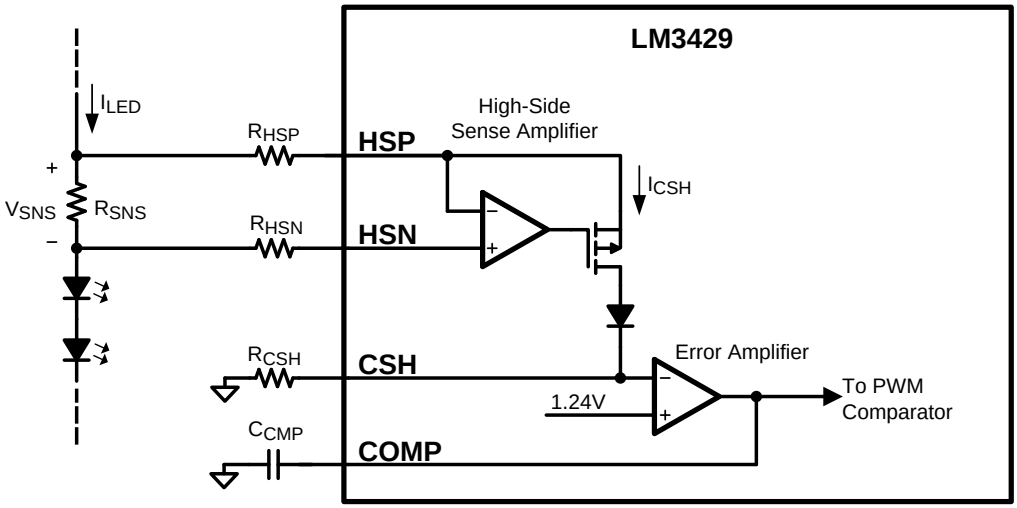


Figure 17. LED Current Sense Circuitry

ANALOG DIMMING

The CSH pin can be used to analog dim the LED current by adjusting the current sense voltage (V_{SNS}). There are several different methods to adjust V_{SNS} using the CSH pin:

1. External variable resistance : Adjust a potentiometer placed in series with R_{CSH} to vary V_{SNS}.
2. External variable current source: Source current (0 µA to I_{CSH}) into the CSH pin to adjust V_{SNS}.

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 18 shows how both methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin since the potentiometer increases the size of the signal current loop.

Method 2 provides a complete dimming range and better noise performance, though it is more complex. It consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer (R_{ADJ}), where R_{ADJ} controls the amount of current sourced into the CSH pin. A higher resistance value will source more current into the CSH pin causing less regulated signal current through R_{HSP}, effectively dimming the LEDs. V_{REF} should be a precise external voltage reference, while Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current (I_{ADD}) sourced into the CSH pin can be calculated:

$$I_{ADD} = \frac{\left(\frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}}\right) - V_{BE\text{-}Q6}}{R_{BIAS}} \quad (10)$$

The corresponding I_{LED} for a specific I_{ADD} is:

$$I_{LED} = \left(I_{CSH} - I_{ADD}\right) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (11)$$

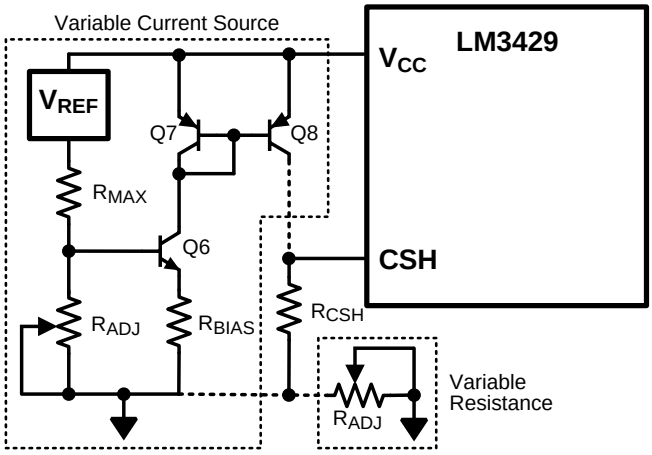


Figure 18. Analog Dimming Circuitry

CURRENT SENSE/CURRENT LIMIT

The LM3429 achieves peak current mode control using a comparator that monitors the MosFET transistor current, comparing it with the COMP pin voltage as shown in Figure 19. Further, it incorporates a cycle-by-cycle over-current protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MosFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 250 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time ($t_{ON\text{-}MIN}$).

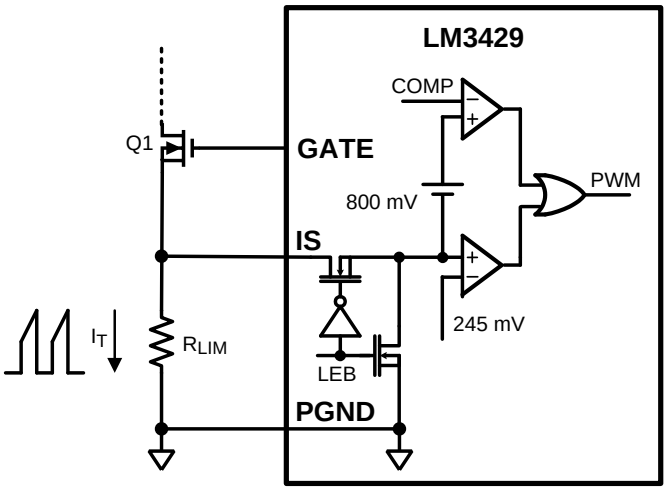


Figure 19. Current Sense / Current Limit Circuitry

There are two possible methods to sense the transistor current. The R_{DS-ON} of the main power MosFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MosFET is in the off state. Alternatively, a sense resistor located in the source of the MosFET may be used for current sensing, however a low inductance (ESL) type is suggested. The cycle-by-cycle current limit (I_{LIM}) can be calulated using either method as the limiting resistance (R_{LIM}):

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} \tag{12}$$

In general, the external series resistor allows for more design flexibility, however it is important to ensure all of the noise sensitive low power ground connections are connected together local to the controller and a single connection is made to the high current PGND (sense resistor ground point).

CONTROL LOOP COMPENSATION

The LM3429 control loop is modeled like any current mode controller. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high frequency pole in the model, however it is above the switching frequency and plays no part in the compensation design process therefore it will be neglected. Since ceramic capacitance is recommended for use with LED drivers due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. Finally, there is a DC gain of the uncompensated loop which is dependent on internal controller gains and the external sensing network.

A buck-boost regulator will be used as an example case. See the Design Guide section for compensation of all topologies.

The uncompensated loop gain for a buck-boost regulator is given by the following equation:

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{13}$$

Where the uncompensated DC loop gain of the system is described as:

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \tag{14}$$

And the output pole (ω_{P1}) is approximated:

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \tag{15}$$

And the right half plane zero (ω_{Z1}) is:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \tag{16}$$

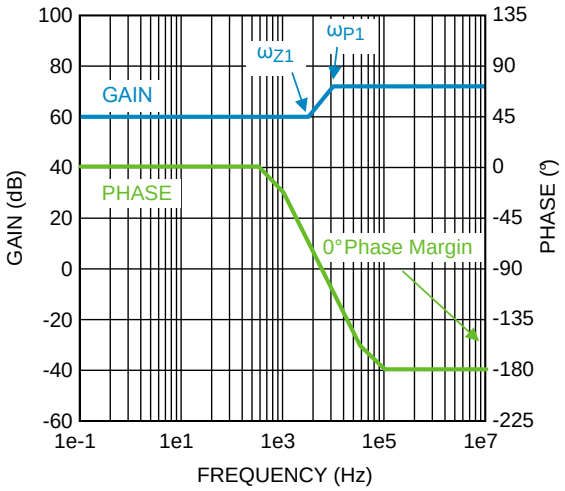


Figure 20. Uncompensated Loop Gain Frequency Response

Figure 20 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while loosing 45°/decade of phase which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high frequency pole (not modeled or shown in figure). The phase will be below -180° at the crossover frequency which means there is no phase margin (180° + phase at crossover frequency) causing system instability. Even if the output pole is below the RHP zero, the phase will still reach -180° before the crossover frequency in most cases yielding instability.

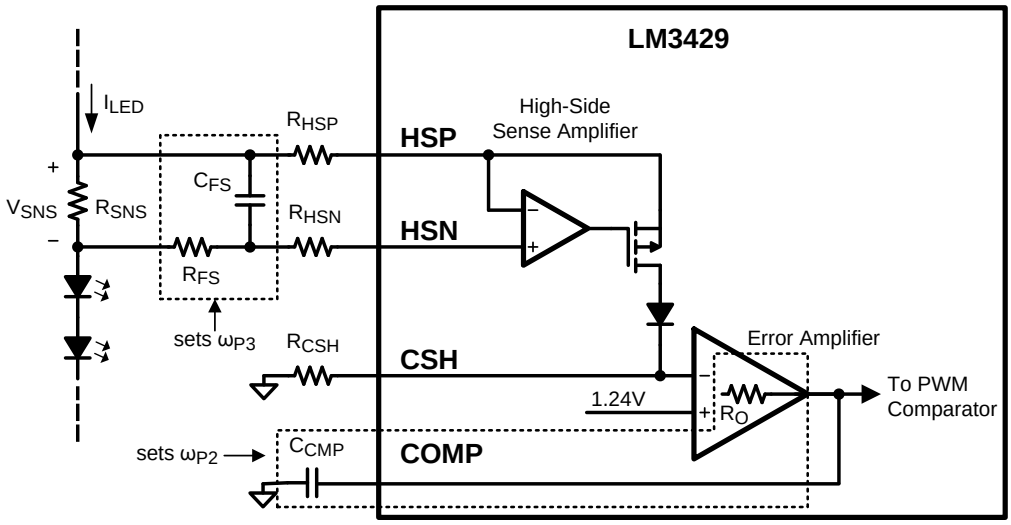


Figure 21. Compensation Circuitry

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin (C_{CMP}) will add a dominant pole to the system, which will ensure adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 20), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant compensation pole (ω_{P2}) is determined by C_{CMP} and the output resistance (R_O) of the error amplifier (typically 5 MΩ):

$$\omega_{P2} = \frac{1}{5e^6 \Omega \times C_{CMP}} \quad (17)$$

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across R_{SNS} to filter the ESL of the sense resistor at the same time. Figure 21 shows how the compensation is physically implemented in the system.

The high frequency pole (ω_{P3}) can be calculated:

$$\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}} \quad (18)$$

The total system transfer function becomes:

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (19)$$

The resulting compensated loop gain frequency response shown in Figure 22 indicates that the system has adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability:

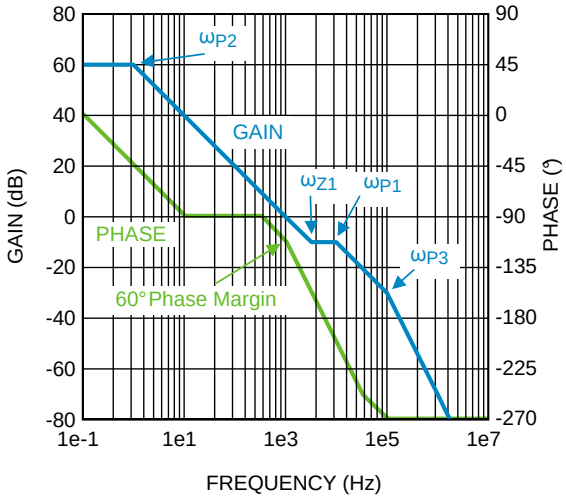


Figure 22. Compensated Loop Gain Frequency Response

OUTPUT OVER-VOLTAGE LOCKOUT (OVLO)

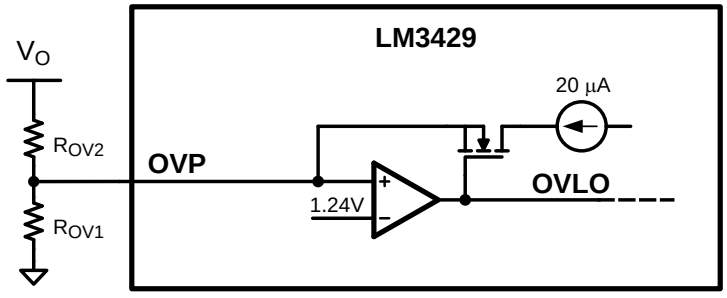


Figure 23. Over-Voltage Protection Circuitry

The LM3429 can be configured to detect an output (or input) over-voltage condition via the OVP pin. The pin features a precision 1.24V threshold with 20 µA (typical) of hysteresis current as shown in Figure 23. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 20 µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage (V_O) should be sensed and translated to ground by using a single PNP as shown in Figure 24.

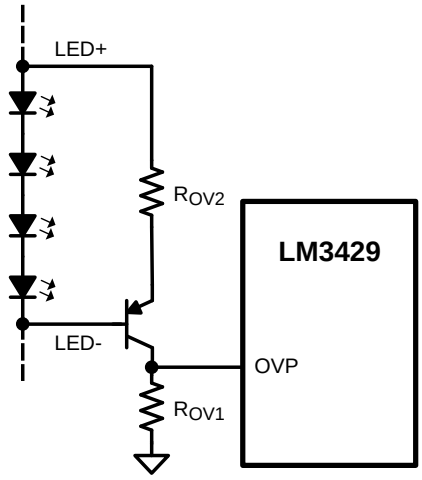


Figure 24. Floating Output OVP Circuitry

The over-voltage turn-off threshold ($V_{TURN-OFF}$) is defined as follows:

Ground Referenced

$$V_{TURN-OFF} = 1.24V \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (20)$$

Floating

$$V_{TURN-OFF} = 1.24V \times \left(\frac{0.5 \times R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (21)$$

In the ground referenced configuration, the voltage across R_{OV2} is V_O - 1.24V whereas in the floating configuration it is V_O - 620 mV where 620 mV approximates the V_{BE} of the PNP transistor.

The over-voltage hysteresis (V_{HYSO}) is defined as follows:

$$V_{HYSO} = 20\,\mu A \times R_{OV2} \quad (22)$$

INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24V threshold with programmable hysteresis as shown in Figure 25. This pin functions as both the PWM dimming input for the LEDs and as a V_{IN} UVLO. When the pin voltage rises and exceeds the 1.24V threshold, 20 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

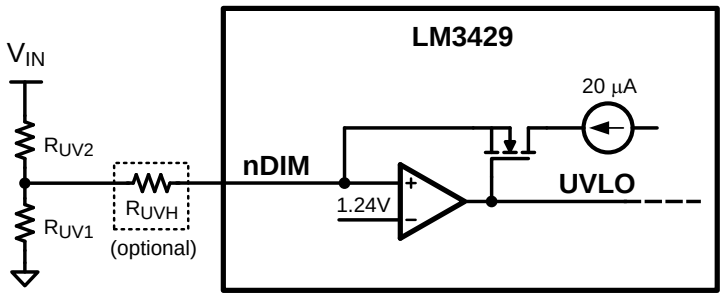


Figure 25. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pull-down MosFET at the nDIM pin (see PWM DIMMING section). In general, at least 3V of hysteresis is necessary when PWM dimming if operating near the UVLO threshold.

The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN\ ON} = 1.24V \times \left(\frac{R_{UV1} + R_{UV2}}{R_{UV1}}\right) \quad (23)$$

The hysteresis (V_{HYS}) is defined as follows:

UVLO only

$$V_{HYS} = 20\,\mu A \times R_{UV2} \quad (24)$$

PWM dimming and UVLO

$$V_{HYS} = 20\,\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}}\right) \quad (25)$$

PWM DIMMING

The active low nDIM pin can be driven with a PWM signal which controls the main NFET (Q1). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, so 30% duty cycle equals approximately 30% LED brightness. This function can be ignored if PWM dimming is not required by using nDIM solely as a V_{IN} UVLO input as described in the INPUT UNDER-VOLTAGE LOCKOUT (UVLO) section or by tying it directly to V_{CC} or V_{IN} (if less than 76VDC).

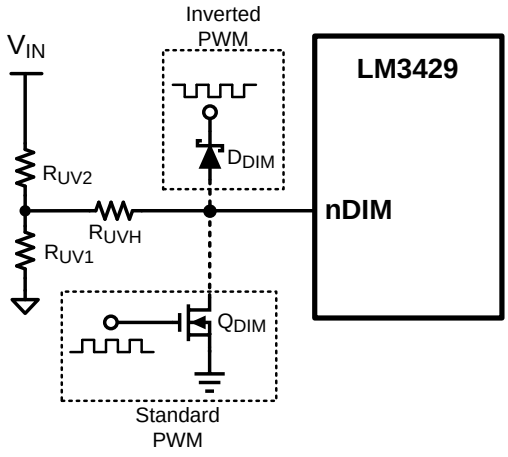


Figure 26. PWM Dimming Circuit

Figure 26 shows two ways the PWM signal can be applied to the nDIM pin:

1. Connect the dimming MosFET (Q_{DIM}) with the drain to the nDIM pin and the source to GND. Apply an external logic-level PWM signal to the gate of Q_{DIM}. A pull down resistor may be necessary to properly turn off Q_{DIM} if no signal is present.
2. Connect the anode of a Schottky diode (D_{DIM}) to the nDIM pin. Apply an external inverted logic-level PWM signal to the cathode of the same diode.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the following condition must be maintained:

$$t_{PULSE} = \frac{2 \times I_{LED} \times V_O \times L1}{V_{IN}^2} \quad (26)$$

In the previous equation, t_{PULSE} is the length of the PWM pulse in seconds.

STARTUP REGULATOR (V_{CC} LDO)

The LM3429 includes a high voltage, low dropout (LDO) bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The V_{CC} output voltage is 6.9V nominally and the supply is internally current limited to 20 mA (minimum). The recommended bypass capacitance range for the V_{CC} regulator is 2.2 µF to 3.3 µF. The output of the V_{CC} regulator is monitored by an internal UVLO circuit that protects the device during startup, normal operation, and shutdown from attempting to operate with insufficient supply voltage.

THERMAL SHUTDOWN

The LM3429 includes thermal shutdown. If the die temperature reaches approximately 165°C the device will shut down (GATE pin low), until it reaches approximately 140°C where it turns on again.

Design Considerations

This section describes the application level considerations when designing with the LM3429. For corresponding calculations, refer to the Design Guide section.

INDUCTOR

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transfered to the load in different ways (as an example, buck-boost operation is detailed in the CURRENT REGULATORS section). The size of the inductor, the voltage across it, and the length of the switching subinterval (t_{ON} or t_{OFF}) determines the inductor current ripple ($\Delta i_{L\text{-}PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L\text{-}PP}$. For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L\text{-}PP}$ is basically equal to the LED ripple current $\Delta i_{LED\text{-}PP}$. However, for boost and buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED\text{-}PP}$, therefore the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}). Therefore, for the buck regulator with no output capacitance, $\Delta i_{L\text{-}PP}$ should also be less than 40% of I_{LED}. For the boost and buck-boost topologies, $\Delta i_{L\text{-}PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L\text{-}PP}$ is suggested to be less than 100% of the average inductor current (I_L) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L\text{-}RMS}$).

LED DYNAMIC RESISTANCE (r_D)

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus R_{SNS}. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (V_{LED}) by the forward current (I_{LED}) leads to an incorrect calculation of the dynamic resistance of a single LED (r_{LED}). The result can be 5 to 10 times higher than the true r_{LED} value.

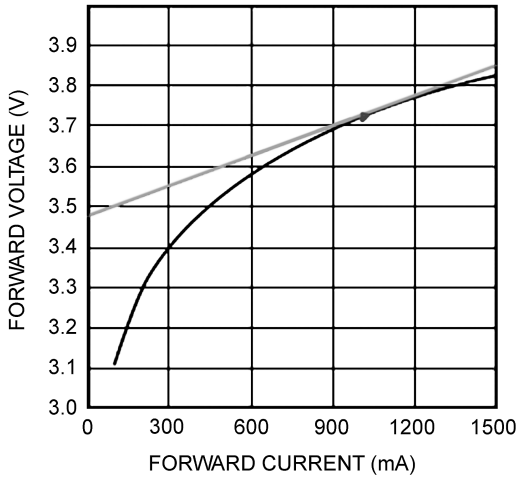


Figure 27. Dynamic Resistance

Obtaining r_{LED} is accomplished by refering to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 27. For any application with more than 2 series LEDs, R_{SNS} can be neglected allowing r_D to be approximated as the number of LEDs multiplied by r_{LED}.

OUTPUT CAPACITOR

For boost and buck-boost regulators, the output capacitor (C_O) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple (Δi_{LED-PP}) below the inductor current ripple (Δi_{L-PP}). In all cases, C_O is sized to provide a desired Δi_{LED-PP}. As mentioned in the INDUCTOR section, Δi_{LED-PP} is recommended by manufacturers to be less than 40% of the average LED current (I_{LED-PP}).

C_O should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

INPUT CAPACITORS

The input capacitance (C_{IN}) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, C_{IN} provides energy during t_{ON} and during t_{OFF}, the input voltage source charges up C_{IN} with the average input current (I_{IN}). For boost regulators, C_{IN} only needs to provide the ripple current due to the direct connection to the inductor. C_{IN} is selected given the maximum input voltage ripple (Δv_{IN-PP}) which can be tolerated. Δv_{IN-PP} is suggested to be less than 10% of the input voltage (V_{IN}).

An input capacitance at least 100% greater than the calculated C_{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

For most applications, it is recommended to bypass the V_{IN} pin with an 0.1 µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the LM3429 device, a 10Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150 kHz filter to eliminate undesired high frequency noise coupling.

N-CHANNEL MosFET (NFET)

The LM3429 requires an external NFET (Q1) as the main power MosFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the NFET on-resistance (R_{DS-ON}).

In general, the NFET should be chosen to minimize total gate charge (Q_g) whenever switching frequencies are high and minimize R_{DS-ON} otherwise. This will minimize the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

RE-CIRCULATING DIODE

A re-circulating diode (D1) is required to carry the inductor current during t_{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

CIRCUIT LAYOUT

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximimize noise rejection and minimize the generation of EMI within the circuit.

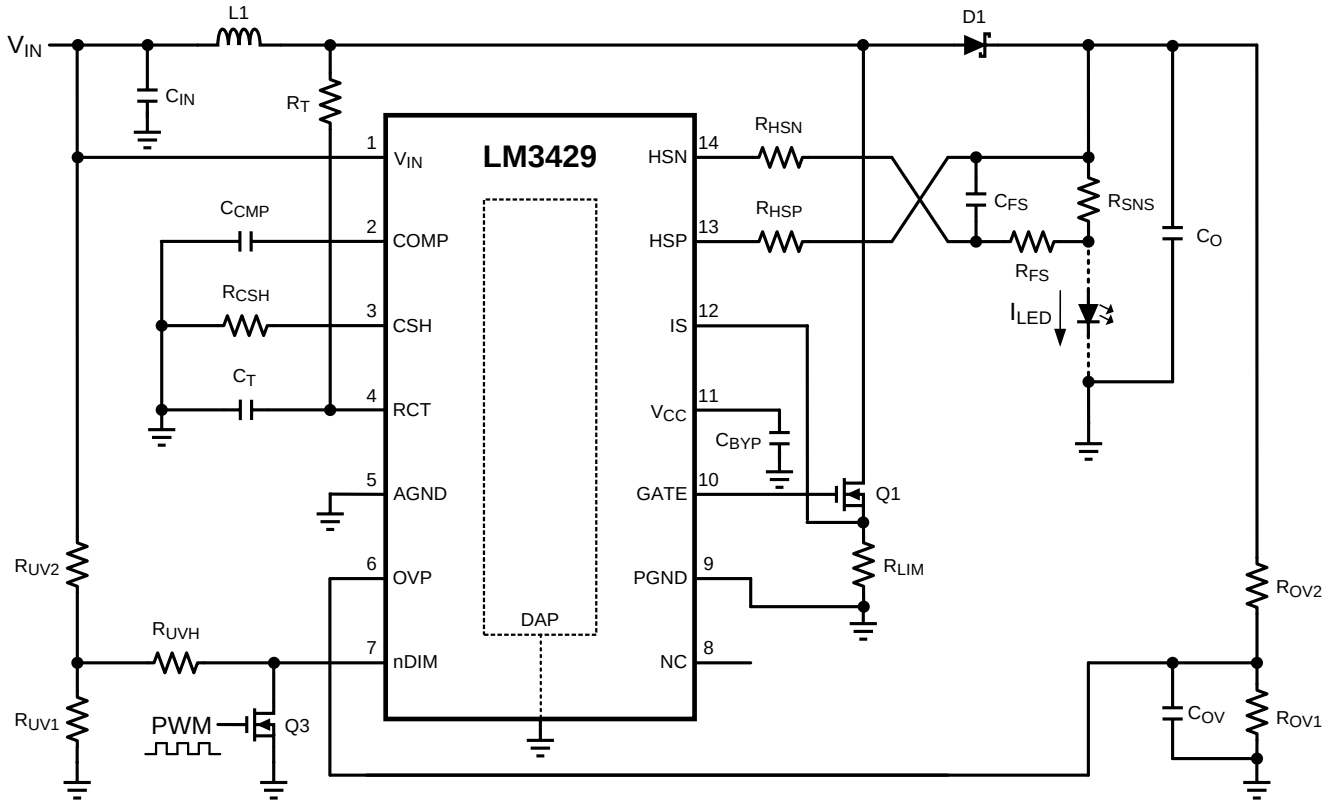
Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM3429 buck regulator contains the input capacitor (C_{IN}), the recirculating diode (D1), the N-channel MosFET (Q1), and the sense resistor (R_{LIM}). In the LM3429 boost and buck-boost regulators, the discontinuous current flows through the output capacitor (C_O), D1, Q1, and R_{LIM}. In either case, this loop should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RCT, COMP, CSH, IS, HSP and HSN pins are all high-impedance inputs which couple external noise easily, therefore the loops containing these nodes should be minimized whenever possible.

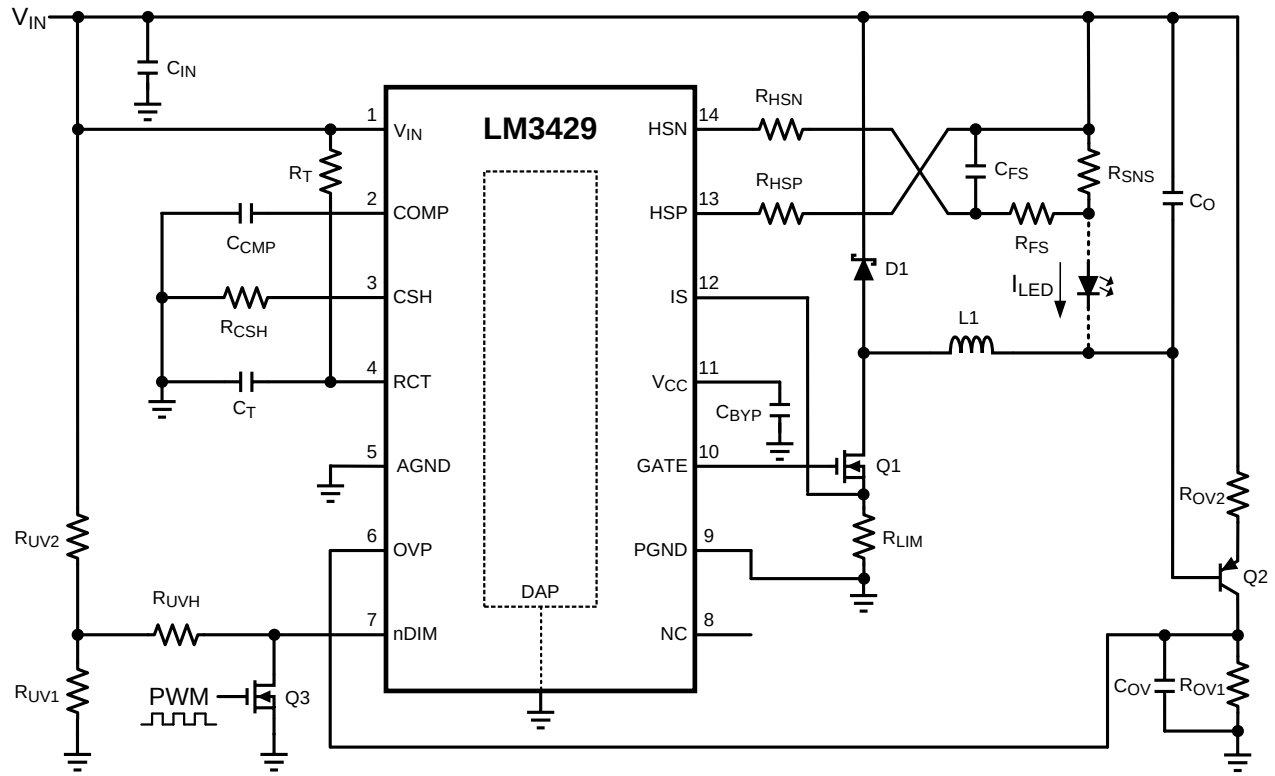
In some applications the LED or LED array can be far away (several inches or more) from the LM3429, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

Basic Topology Schematics

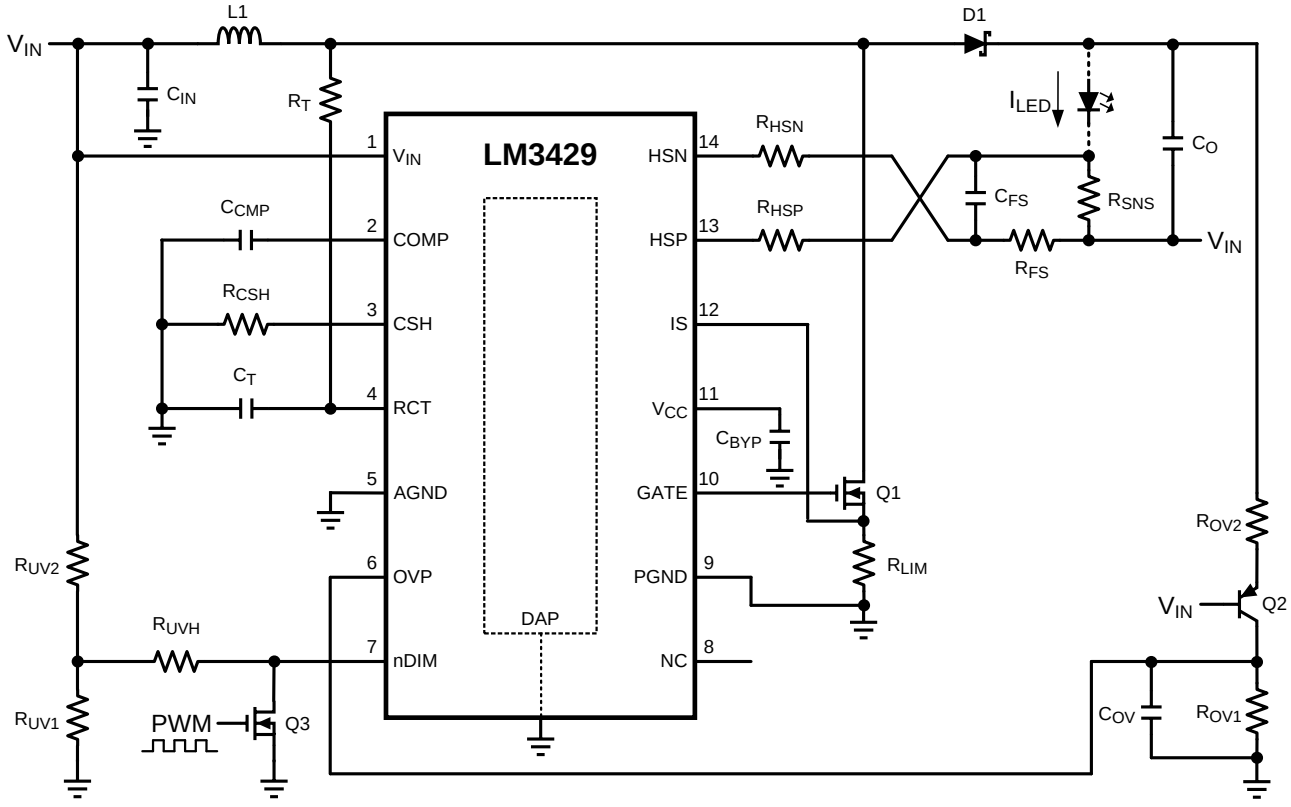
BOOST REGULATOR (V_{IN} < V_O)



BUCK REGULATOR (V_{IN} > V_O)



BUCK-BOOST REGULATOR



Design Guide

Refer to Basic Topology Schematics section.

SPECIFICATIONS

Number of series LEDs: N

Single LED forward voltage: V_{LED}

Single LED dynamic resistance: r_{LED}

Nominal input voltage: V_{IN}

Input voltage range: V_{IN-MAX}, V_{IN-MIN}

Switching frequency: f_{SW}

Current sense voltage: V_{SNS}

Average LED current: I_{LED}

Inductor current ripple: Δi_{L-PP}

LED current ripple: Δi_{LED-PP}

Peak current limit: I_{LIM}

Input voltage ripple: Δv_{IN-PP}

Output OVLO characteristics: $V_{TURN-OFF}$, V_{HYSO}

Input UVLO characteristics: $V_{TURN-ON}$, V_{HYS}

1. OPERATING POINT

Given the number of series LEDs (N), the forward voltage (V_{LED}) and dynamic resistance (r_{LED}) for a single LED, solve for the nominal output voltage (V_O) and the nominal LED string dynamic resistance (r_D):

$$V_O = N \times V_{LED} \tag{27}$$

$$r_D = N \times r_{LED} \tag{28}$$

Solve for the ideal nominal duty cycle (D):

Buck

$$D = \frac{V_O}{V_{IN}} \tag{29}$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \tag{30}$$

Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \tag{31}$$

Using the same equations, find the minimum duty cycle (D_{MIN}) using maximum input voltage (V_{IN-MAX}) and the maximum duty cycle (D_{MAX}) using the minimum input voltage (V_{IN-MIN}). Also, remember that D' = 1 - D.

2. SWITCHING FREQUENCY

Set the switching frequency (f_{SW}) by assuming a C_T value of 1 nF and solving for R_T:

Buck (Constant Ripple vs. V_{IN})

$$R_T = \frac{25 \times (V_{IN} - V_O)}{f_{SW} \times C_T \times V_{IN}} \quad (32)$$

Buck (Constant Ripple vs. V_O)

$$R_T = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{f_{SW} \times C_T \times V_{IN}^2} \quad (33)$$

Boost and Buck-boost

$$R_T = \frac{25}{f_{SW} \times C_T} \quad (34)$$

3. AVERAGE LED CURRENT

For all topologies, set the average LED current (I_{LED}) knowing the desired current sense voltage (V_{SNS}) and solving for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \quad (35)$$

If the calculated R_{SNS} is too far from a desired standard value, then V_{SNS} will have to be adjusted to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming R_{CSH} = 12.4 kΩ and solving for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \quad (36)$$

If the calculated R_{HSP} is too far from a desired standard value, then R_{CSH} can be adjusted to obtain a standard value.

4. INDUCTOR RIPPLE CURRENT

Set the nominal inductor ripple current ($\Delta i_{L\text{-}PP}$) by solving for the appropriate inductor (L1):

Buck

$$L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} \quad (37)$$

Boost and Buck-boost

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} \quad (38)$$

To set the worst case inductor ripple current, use $V_{IN\text{-}MAX}$ and D_{MIN} when solving for L1.

The minimum allowable inductor RMS current rating ($I_{L\text{-}RMS}$) can be calculated as:

Buck

$$I_{L\text{-}RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP}}{I_{LED}}\right)^2} \quad (39)$$

Boost and Buck-boost

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP} \times D'}{I_{LED}} \right)^2} \quad (40)$$

5. LED RIPPLE CURRENT

Set the nominal LED ripple current ($\Delta i_{LED\text{-}PP}$), by solving for the output capacitance (C_O):

Buck

$$C_O = \frac{\Delta i_{L\text{-}PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED\text{-}PP}} \quad (41)$$

Boost and Buck-boost

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}} \quad (42)$$

To set the worst case LED ripple current, use D_{MAX} when solving for C_O.

The minimum allowable RMS output capacitor current rating ($I_{CO\text{-}RMS}$) can be approximated:

Buck

$$I_{CO\text{-}RMS} = \frac{\Delta i_{LED\text{-}PP}}{\sqrt{12}} \quad (43)$$

Boost and Buck-boost

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1\text{-}D_{MAX}}} \quad (44)$$

6. PEAK CURRENT LIMIT

Set the peak current limit (I_{LIM}) by solving for the transistor path sense resistor (R_{LIM}):

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} \quad (45)$$

7. LOOP COMPENSATION

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain (T_U) of the regulator can be approximated:

Buck

$$T_U = T_{U0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (46)$$

Boost and Buck-boost

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{47}$$

Where the pole (ω_{P1}) is approximated:

Buck

$$\omega_{P1} = \frac{1}{r_D \times C_O} \tag{48}$$

Boost

$$\omega_{P1} = \frac{2}{r_D \times C_O} \tag{49}$$

Buck-boost

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \tag{50}$$

And the RHP zero (ω_{Z1}) is approximated:

Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{L1} \tag{51}$$

Buck-boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \tag{52}$$

And the uncompensated DC loop gain (T_{U0}) is approximated:

Buck

$$T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \tag{53}$$

Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \tag{54}$$

Buck-boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \tag{55}$$

For all topologies, the primary method of compensation is to place a low frequency dominant pole (ω_{P2}) which will ensure that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor (C_{CMP}) from the COMP pin to GND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} \tag{56}$$

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5e^{6}} \quad (57)$$

If analog dimming is used, C_{CMP} should be approximately 4x larger to maintain stability as the LEDs are dimmed to zero.

A high frequency compensation pole (ω_{P3}) can be used to attenuate switching noise and provide better gain margin. Assuming R_{FS} = 10Ω, C_{FS} is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

$$\omega_{P3} = \max(\omega_{P1}, \omega_{Z1}) \times 10 \quad (58)$$

$$C_{FS} = \frac{1}{10 \times \omega_{P3}} \quad (59)$$

The total system loop gain (T) can then be written as:

Buck

$$T = T_{U0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (60)$$

Boost and Buck-boost

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (61)$$

8. INPUT CAPACITANCE

Set the nominal input voltage ripple (Δv_{IN-PP}) by solving for the required capacitance (C_{IN}):

Buck

$$C_{IN} = \frac{I_{LED} \times (1 - D) \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (62)$$

Boost

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \quad (63)$$

Buck-boost

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (64)$$

Use D_{MAX} to set the worst case input voltage ripple, when solving for C_{IN} in a buck-boost regulator and D_{MID} = 0.5 when solving for C_{IN} in a buck regulator.

The minimum allowable RMS input current rating ($I_{CIN-RMS}$) can be approximated:

Buck

$$I_{CIN-RMS} = I_{LED} \times \sqrt{D_{MID} \times (1 - D_{MID})} \quad (65)$$

Boost

$$I_{CIN\text{-}RMS} = \frac{\Delta i_{L\text{-}PP}}{\sqrt{12}} \quad (66)$$

Buck-boost

$$I_{CIN\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1\text{-}D_{MAX}}} \quad (67)$$

9. NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage ($V_{T\text{-}MAX}$):

Buck

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} \quad (68)$$

Boost

$$V_{T\text{-}MAX} = V_O \quad (69)$$

Buck-boost

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (70)$$

The current rating should be at least 10% higher than the maximum average NFET current ($I_{T\text{-}MAX}$):

Buck

$$I_{T\text{-}MAX} = D_{MAX} \times I_{LED} \quad (71)$$

Boost and Buck-boost

$$I_{T\text{-}MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} \quad (72)$$

Approximate the nominal RMS transistor current ($I_{T\text{-}RMS}$) :

Buck

$$I_{T\text{-}RMS} = I_{LED} \times \sqrt{D} \quad (73)$$

Boost and Buck-boost

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} \quad (74)$$

Given an NFET with on-resistance ($R_{DS\text{-}ON}$), solve for the nominal power dissipation (P_T):

$$P_T = I_{T\text{-}RMS}^2 \times R_{DSON} \quad (75)$$

10. DIODE

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ($V_{RD\text{-}MAX}$):

Buck

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} \quad (76)$$

Boost

$$V_{RD\text{-}MAX} = V_O \quad (77)$$

Buck-boost

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (78)$$

The current rating should be at least 10% higher than the maximum average diode current ($I_{D\text{-}MAX}$):

Buck

$$I_{D\text{-}MAX} = (1 - D_{MIN}) \times I_{LED} \quad (79)$$

Boost and Buck-boost

$$I_{D\text{-}MAX} = I_{LED} \quad (80)$$

Replace D_{MAX} with D in the $I_{D\text{-}MAX}$ equation to solve for the average diode current (I_D). Given a diode with forward voltage (V_{FD}), solve for the nominal power dissipation (P_D):

$$P_D = I_D \times V_{FD} \quad (81)$$

11. OUTPUT OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ($V_{TURN\text{-}OFF}$) and the desired hysteresis (V_{HYSO}). To set V_{HYSO}, solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} \quad (82)$$

To set $V_{TURN\text{-}OFF}$, solve for R_{OV1}:

Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 1.24V} \quad (83)$$

Buck-boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 620\,mV} \quad (84)$$

A small filter capacitor (C_{OVP} = 47 pF) should be added from the OVP pin to ground to reduce coupled switching noise.

12. INPUT UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ($V_{TURN\text{-}ON}$) and the desired hysteresis (V_{HYS}).

Method #1: If no PWM dimming is required, a two resistor network can be used. To set V_{HYS}, solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} \quad (85)$$

To set $V_{TURN\text{-}ON}$, solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} \quad (86)$$

Method #2: If PWM dimming is required, a three resistor network is suggested. To set $V_{TURN-ON}$, assume R_{UV2} = 10 kΩ and solve for R_{UV1} as in Method #1. To set V_{HYS}, solve for R_{UVH}:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 20\,\mu A \times R_{UV2})}{20\,\mu A \times (R_{UV1} + R_{UV2})} \quad (87)$$

13. PWM DIMMING METHOD

PWM dimming can be performed several ways:

Method #1: Connect the dimming MosFET (Q_3) with the drain to the nDIM pin and the source to GND. Apply an external PWM signal to the gate of Q_{DIM}. A pull down resistor may be necessary to properly turn off Q_3.

Method #2: Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

14. ANALOG DIMMING METHOD

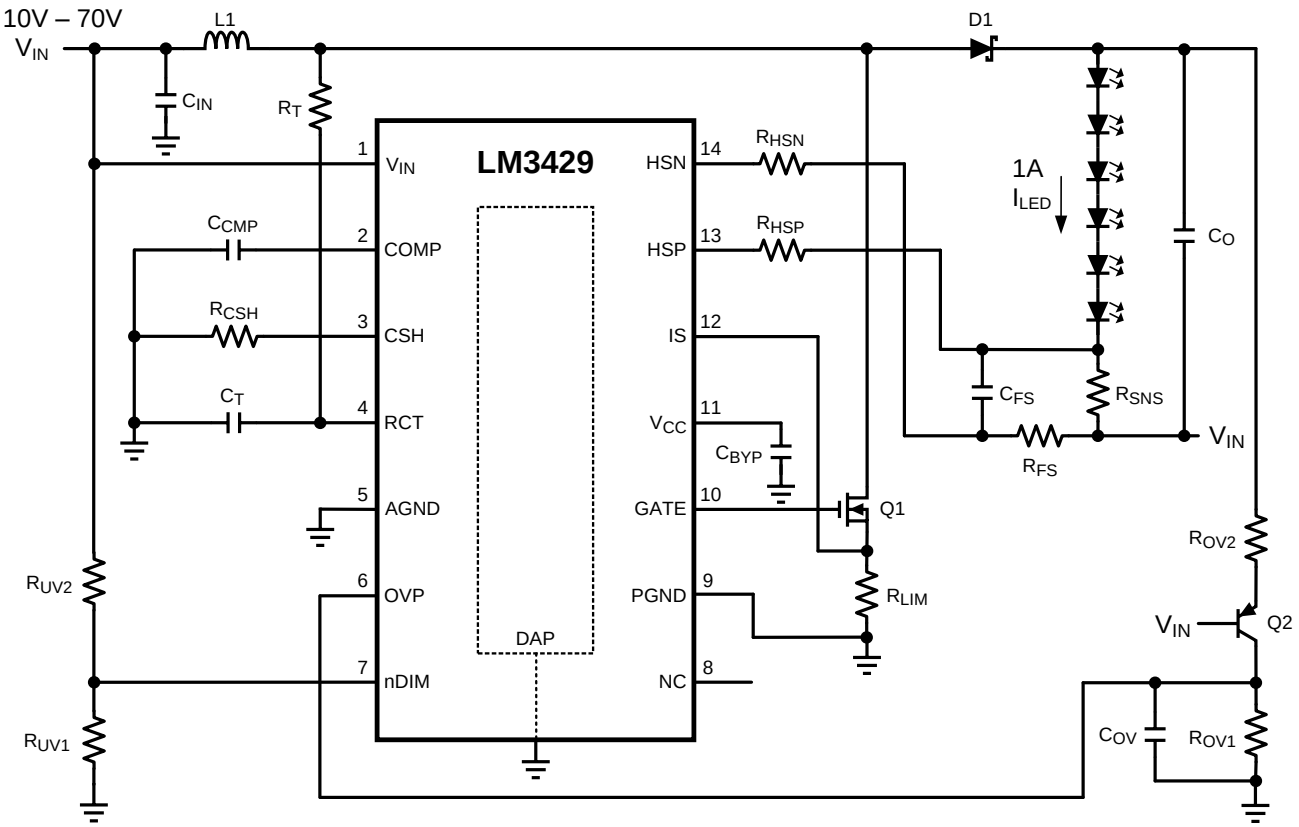
Analog dimming can be performed several ways:

Method #1: Place a potentiometer in series with the R_{CSH} resistor to dim the LED current from the nominal I_{LED} to near zero.

Method #2: Connect a controlled current source as detailed in the ANALOG DIMMING section to the CSH pin. Increasing the current sourced into the CSH node will decrease the LEDs from the nominal I_{LED} to zero current.

Design Example #1

BUCK-BOOST APPLICATION - 6 LEDs at 1A



SPECIFICATIONS

N = 6

V_{LED} = 3.5V

r_{LED} = 325 mΩ

V_{IN} = 24V

V_{IN-MIN} = 10V

V_{IN-MAX} = 70V

f_{SW} = 700 kHz

V_{SNS} = 100 mV

I_{LED} = 1A

Δi_{L-PP} = 500 mA

Δi_{LED-PP} = 50 mA

Δv_{IN-PP} = 1V

I_{LIM} = 6A

$V_{TURN-ON}$ = 10V

V_{HYS} = 3V

$V_{TURN-OFF}$ = 40V

V_{HYSO} = 10V

1. OPERATING POINT

Solve for V_O and r_D:

$$V_O = N \times V_{LED} = 6 \times 3.5V = 21V \quad (88)$$

$$r_D = N \times r_{LED} = 6 \times 325\ m\Omega = 1.95\Omega \quad (89)$$

Solve for D, D', D_{MAX}, and D_{MIN}:

$$D = \frac{V_O}{V_O + V_{IN}} = \frac{21V}{21V + 24V} = 0.467 \quad (90)$$

$$D' = 1 - D = 1 - 0.467 = 0.533 \quad (91)$$

$$D_{MIN} = \frac{V_O}{V_O + V_{IN-MAX}} = \frac{21V}{21V + 70V} = 0.231 \quad (92)$$

$$D_{MAX} = \frac{V_O}{V_O + V_{IN-MIN}} = \frac{21V}{21V + 10V} = 0.677 \quad (93)$$

2. SWITCHING FREQUENCY

Assume C_T = 1 nF and solve for R_T:

$$R_T = \frac{25}{f_{SW} \times C_T} = \frac{25}{700\ kHz \times 1\ nF} = 35.7\ k\Omega \quad (94)$$

The closest standard resistor is actually 35.7 kΩ therefore the f_{SW} is:

$$f_{SW} = \frac{25}{R_T \times C_T} = \frac{25}{35.7\ k\Omega \times 1\ nF} = 700\ kHz \quad (95)$$

The chosen components from step 2 are:

$$\boxed{\begin{aligned} C_T &= 1\ \text{nF} \\ R_T &= 35.7\ \text{k}\Omega \end{aligned}} \tag{96}$$

3. AVERAGE LED CURRENT

Solve for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} = \frac{100\ \text{mV}}{1\text{A}} = 0.1\Omega \tag{97}$$

Assume R_{CSH} = 12.4 kΩ and solve for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24\text{V}} = \frac{1\text{A} \times 12.4\ \text{k}\Omega \times 0.1\Omega}{1.24\text{V}} = 1.0\ \text{k}\Omega \tag{98}$$

The closest standard resistor for R_{SNS} is actually 0.1Ω and for R_{HSP} is actually 1 kΩ therefore I_{LED} is:

$$I_{LED} = \frac{1.24\text{V} \times R_{HSP}}{R_{SNS} \times R_{CSH}} = \frac{1.24\text{V} \times 1.0\ \text{k}\Omega}{0.1\Omega \times 12.4\ \text{k}\Omega} = 1.0\text{A} \tag{99}$$

The chosen components from step 3 are:

$$\boxed{\begin{aligned} R_{SNS} &= 0.1\Omega \\ R_{CSH} &= 12.4\ \text{k}\Omega \\ R_{HSP} &= R_{HSN} = 1\text{k}\Omega \end{aligned}} \tag{100}$$

4. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$\text{L1} = \frac{V_{IN} \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} = \frac{24\text{V} \times 0.467}{500\ \text{mA} \times 700\ \text{kHz}} = 32\ \mu\text{H} \tag{101}$$

The closest standard inductor is 33 µH therefore the actual $\Delta i_{L\text{-}PP}$ is:

$$\Delta i_{L\text{-}PP} = \frac{V_{IN} \times D}{\text{L1} \times f_{SW}} = \frac{24\text{V} \times 0.467}{33\ \mu\text{H} \times 700\ \text{kHz}} = 485\ \text{mA} \tag{102}$$

Determine minimum allowable RMS current rating:

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L\text{-}PP} \times D'}{I_{LED}}\right)^2}$$

$$I_{L\text{-}RMS} = \frac{1\text{A}}{0.533} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{485\ \text{mA} \times 0.533}{1\text{A}}\right)^2}$$

$$I_{L\text{-}RMS} = 1.88\text{A} \tag{103}$$

The chosen component from step 4 is:

$$\boxed{\text{L1} = 33\ \mu\text{H}} \tag{104}$$

5. OUTPUT CAPACITANCE

Solve for C_O:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}}$$

$$C_O = \frac{1A \times 0.467}{1.95\Omega \times 50\ mA \times 700\ kHz} = 6.84\,\mu F \quad (105)$$

The closest standard capacitor is 6.8 µF therefore the actual $\Delta i_{LED\text{-}PP}$ is:

$$\Delta i_{LED\text{-}PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED\text{-}PP} = \frac{1A \times 0.467}{1.95\Omega \times 6.8\mu F \times 700\ kHz} = 50\ mA \quad (106)$$

Determine minimum allowable RMS current rating:

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \quad (107)$$

The chosen components from step 5 are:

$$\boxed{C_O = 6.8\mu F} \quad (108)$$

6. PEAK CURRENT LIMIT

Solve for R_{LIM}:

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} = \frac{245\ mV}{6A} = 0.041\Omega \quad (109)$$

The closest standard resistor is 0.04 Ω therefore I_{LIM} is:

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} = \frac{245\ mV}{0.04\Omega} = 6.13A \quad (110)$$

The chosen component from step 6 is:

$$\boxed{R_{LIM} = 0.04\Omega} \quad (111)$$

7. LOOP COMPENSATION

ω_{P1} is approximated:

$$\omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 6.8\ \mu F} = 110k\frac{rad}{sec} \quad (112)$$

ω_{Z1} is approximated:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\mu H} = 37k\frac{rad}{sec} \quad (113)$$

T_{U0} is approximated:

$$T_{U0} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \quad (114)$$

To ensure stability, calculate ω_{P2}:

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{Z1}}{5 \times 5630} = \frac{37k\frac{rad}{sec}}{5 \times 5630} = 1.173\frac{rad}{sec} \quad (115)$$

Solve for C_{CMP}:

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5e^6\Omega} = \frac{1}{1.173 \frac{rad}{sec} \times 5e^6\Omega} = 0.17\,\mu F \tag{116}$$

To attenuate switching noise, calculate ω_{P3}:

$$\omega_{P3} = \max \omega_{P1}, \omega_{Z1} \times 10 = \omega_{P1} \times 10$$

$$\omega_{P3} = 110k \frac{rad}{sec} \times 10 = 1.1M \frac{rad}{sec} \tag{117}$$

Assume R_{FS} = 10Ω and solve for C_{FS}:

$$C_{FS} = \frac{1}{10\Omega \times \omega_{P3}} = \frac{1}{10\Omega \times 1.1M \frac{rad}{sec}} = 0.091\,\mu F \tag{118}$$

The chosen components from step 7 are:

$$\boxed{\begin{array}{l} C_{COMP} = 0.22\,\mu F \\ R_{FS} = 10\Omega \\ C_{FS} = 0.1\,\mu F \end{array}} \tag{119}$$

8. INPUT CAPACITANCE

Solve for the minimum C_{IN}:

$$C_{IN} = \frac{I_{LED} \times D}{\Delta v_{IN-PP} \times f_{SW}} = \frac{1A \times 0.467}{100\,mV \times 700\,kHz} = 6.66\,\mu F \tag{120}$$

To minimize power supply interaction a 200% larger capacitance of approximately 14 µF is used, therefore the actual Δv_{IN-PP} is much lower. Since high voltage ceramic capacitor selection is limited, three 4.7 µF X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

$$I_{IN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \tag{121}$$

The chosen components from step 8 are:

$$\boxed{C_{IN} = 3 \times 4.7\,\mu F} \tag{122}$$

9. NFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \tag{123}$$

$$I_{T-MAX} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \tag{124}$$

A 100V NFET is chosen with a current rating of 32A due to the low R_{DS-ON} = 50 mΩ. Determine I_{T-RMS} and P_T:

$$I_{T-RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \tag{125}$$

$$P_T = I_{T-RMS}^2 \times R_{DSON} = 1.28A^2 \times 50\,m\Omega = 82\,mW \tag{126}$$

The chosen component from step 9 is:

$$\boxed{Q1 \rightarrow 32A,\ 100V,\ DPAK} \tag{127}$$

10. DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O = 70V + 21V = 91V \tag{128}$$

$$I_{D\text{-}MAX} = I_{LED} = 1A \tag{129}$$

A 100V diode is chosen with a current rating of 12A and V_D = 600 mV. Determine P_D:

$$P_D = I_D \times V_{FD} = 1A \times 600\ mV = 600\ mW \tag{130}$$

The chosen component from step 10 is:

$$\boxed{D1 \rightarrow 12A,\ 100V,\ DPAK} \tag{131}$$

11. INPUT UVLO

Solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} = \frac{3V}{20\,\mu A} = 150\,k\Omega \tag{132}$$

The closest standard resistor is 150 kΩ therefore V_{HYS} is:

$$V_{HYS} = R_{UV2} \times 20\,\mu A = 150\,k\Omega \times 20\,\mu A = 3V \tag{133}$$

Solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} = \frac{1.24V \times 150\,k\Omega}{10V - 1.24V} = 21.2\,k\Omega \tag{134}$$

The closest standard resistor is 21 kΩ making $V_{TURN\text{-}ON}$:

$$V_{TURN\text{-}ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN\text{-}ON} = \frac{1.24V \times (21\,k\Omega + 150\,k\Omega)}{21\,k\Omega} = 10.1V \tag{135}$$

The chosen components from step 11 are:

$$\boxed{\begin{aligned} R_{UV1} &= 21\,k\Omega \\ R_{UV2} &= 150\,k\Omega \end{aligned}} \tag{136}$$

12. OUTPUT OVLO

Solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} = \frac{10V}{20\,\mu A} = 500\,k\Omega \tag{137}$$

The closest standard resistor is 499 kΩ therefore V_{HYSO} is:

$$V_{HYSO} = R_{OV2} \times 20\,\mu A = 499\,k\Omega \times 20\,\mu A = 9.98V \tag{138}$$

Solve for R_{OV1}:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 0.62V} = \frac{1.24V \times 499k\Omega}{40V - 0.62V} = 15.7k\Omega \quad (139)$$

The closest standard resistor is 15.8 kΩ making $V_{TURN\text{-}OFF}$:

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}$$

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times 15.8\ k\Omega + 499\ k\Omega)}{15.8\ k\Omega} = 39.8V \quad (140)$$

The chosen components from step 12 are:

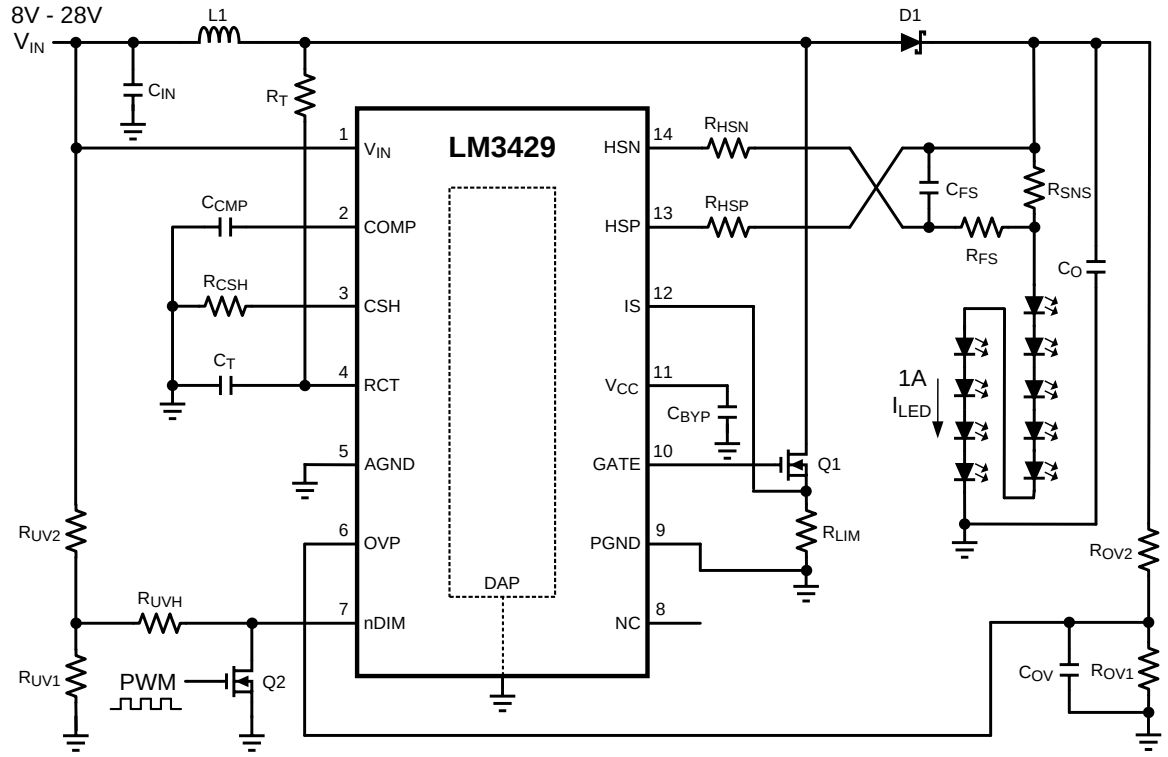
R_{OV1} = 15.8 kΩ
R_{OV2} = 499 kΩ (141)

Design #1 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	0.22 µF X7R 10% 25V	MURATA	GRM21BR71E224KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
3	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
1	C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	33 µH 20% 6.3A	COILCRAFT	MSS1278-333MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	21 kΩ 1%	VISHAY	CRCW080521K0FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA

APPLICATIONS INFORMATION

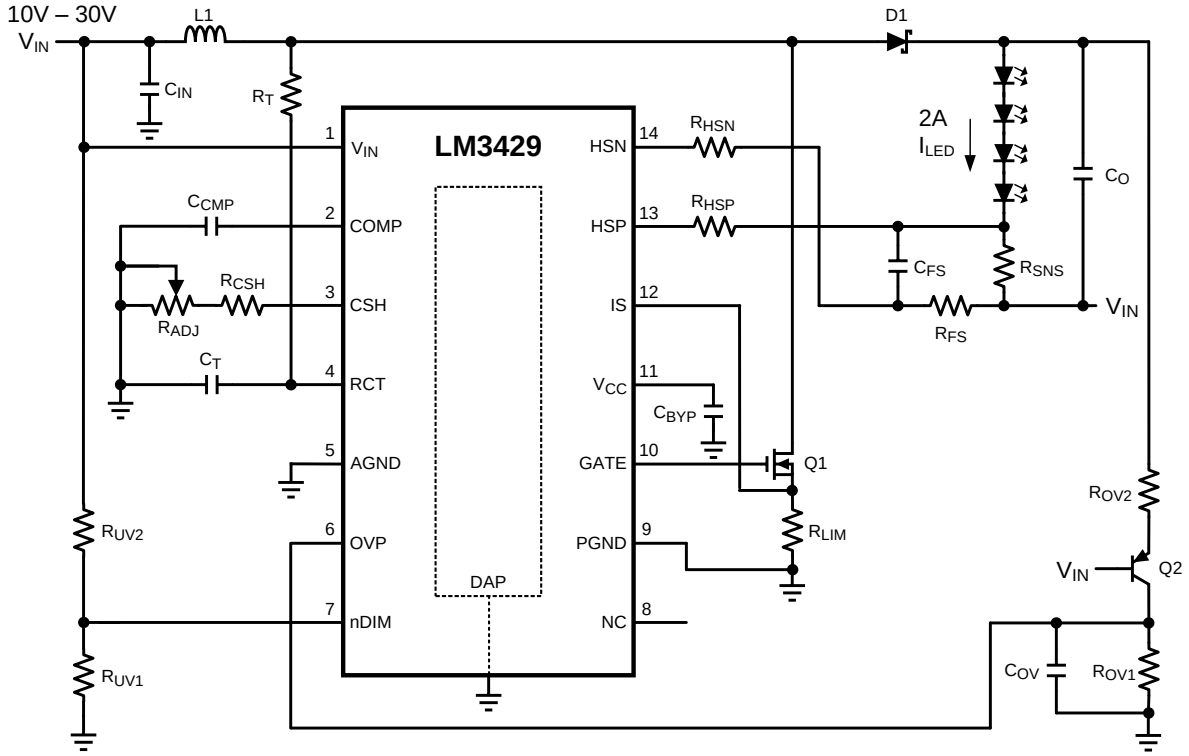
DESIGN #2: BOOST PWM DIMMING APPLICATION - 9 LEDs at 1A



Design #2 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
2	C_{CMP}, C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
2, 1	C_{IN}, C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	33 µH 20% 6.3A	COILCRAFT	MSS1278-333MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	NMOS 60V 115 mA	ON SEMI	2N7002ET1G
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.06Ω 1% 1W	VISHAY	WSL2512R0600FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	1.82 kΩ 1%	VISHAY	CRCW08051K82FKEA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510KFKEA
1	R_{UVH}	17.8 kΩ 1%	VISHAY	CRCW080517K8FKEA

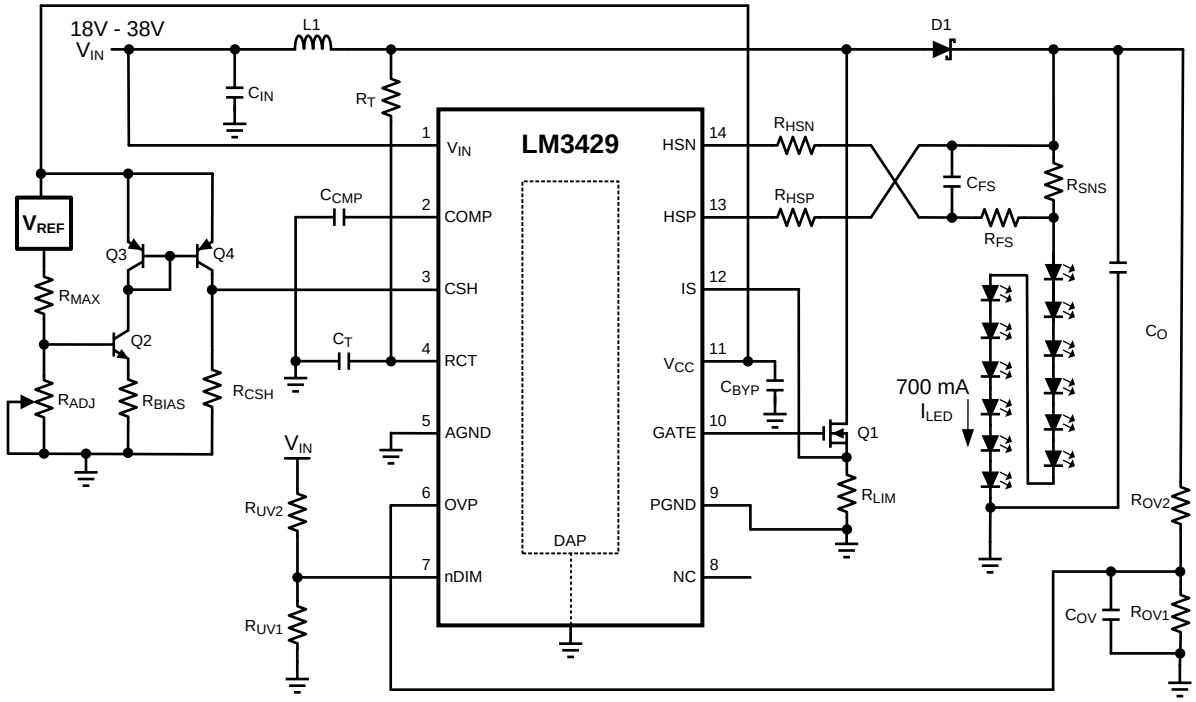
DESIGN #3: BUCK-BOOST ANALOG DIMMING APPLICATION - 4 LEDs at 2A



Design #3 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	1.0 µF X7R 10% 10V	MURATA	GRM21BR71A105KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 50V	MURATA	GRM21BR71E104KA01L
2, 1	C_{IN}, C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60V 5A	VISHAY	CDBC560-G
1	L1	22 µH 20% 7.2A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{ADJ}	1.0 MΩ potentiometer	BOURNS	3352P-1-105
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	18.2 kΩ 1%	VISHAY	CRCW080518K2FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.05Ω 1% 1W	VISHAY	WSL2512R0500FEA
1	R_T	41.2 kΩ 1%	VISHAY	CRCW080541K2FKEA
1	R_{UV1}	21 kΩ 1%	VISHAY	CRCW080521K0FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA

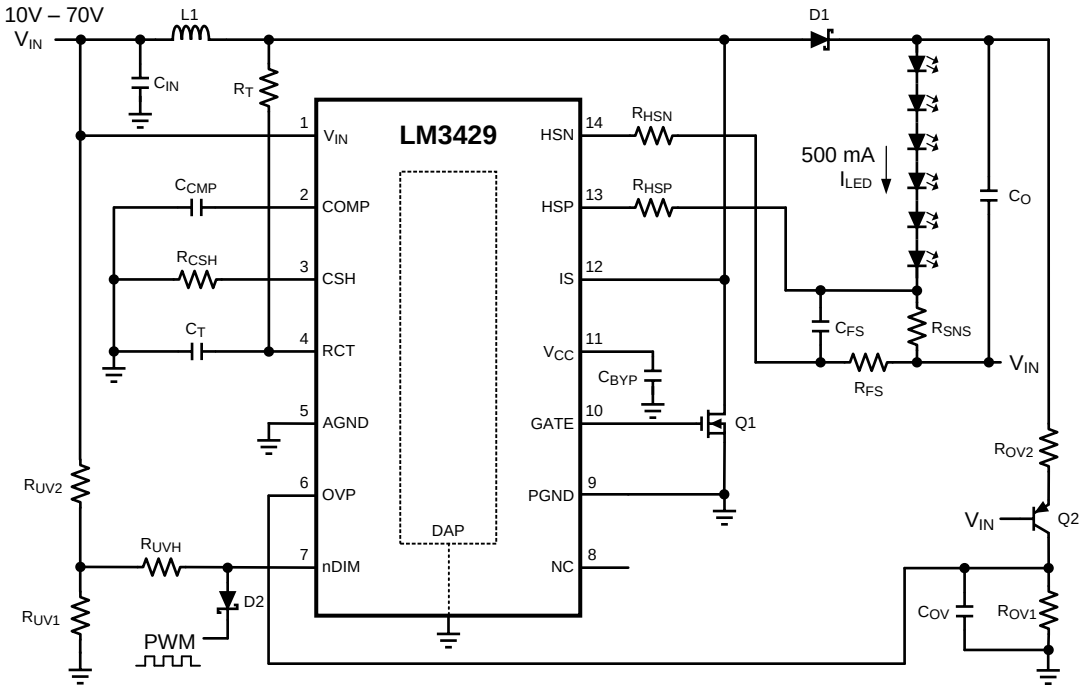
DESIGN #4: BOOST ANALOG DIMMING APPLICATION - 12 LEDs at 700mA



Design #4 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	1.0 µF X7R 10% 10V	MURATA	GRM21BR71A105KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 50V	MURATA	GRM21BR71E104KA01L
2, 1	C_{IN}, C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	47 µH 20% 5.3A	COILCRAFT	MSS1278-473MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	NPN 40V 200 mA	FAIRCHILD	MMBT3904
1	Q3, Q4 (dual pack)	Dual PNP 40V 200 mA	FAIRCHILD	FFB3906
1	R_{ADJ}	100 kΩ potentiometer	BOURNS	3352P-1-104
1	R_{BIAS}	40.2 kΩ 1%	VISHAY	CRCW080540K2FKEA
1	R_{CSH}, R_{OV1}, R_{UV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.05 kΩ 1%	VISHAY	CRCW08051K05FKEA
1	R_{LIM}	0.06Ω 1% 1W	VISHAY	WSL2512R0600FEA
1	R_{MAX}	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.15Ω 1% 1W	VISHAY	WSL2512R1500FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA
1	V_{REF}	5V precision reference	TI	LM4040

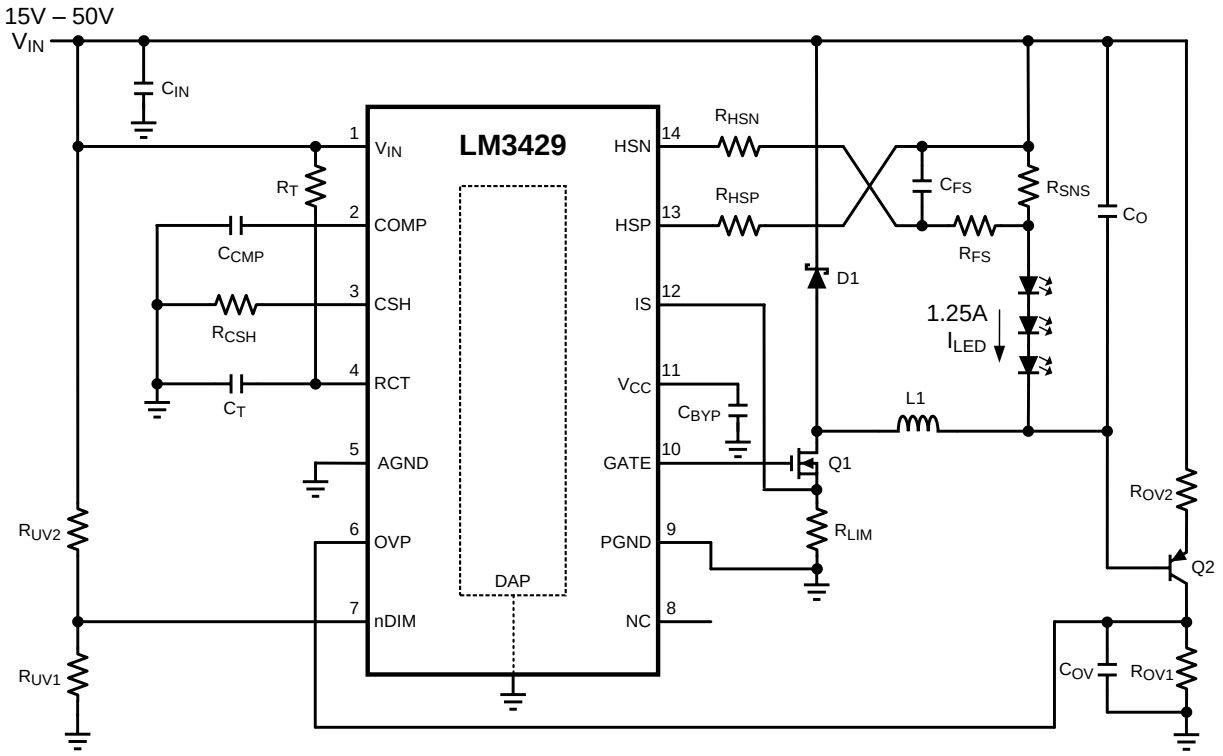
DESIGN #5: BUCK-BOOST PWM DIMMING APPLICATION - 6 LEDs at 500mA



Design #5 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	0.68 µF X7R 10% 25V	MURATA	GRM21BR71E684KA88L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
3	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
1	C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	D2	Schottky 30V 500 mA	ON SEMI	BAT54T1G
1	L1	68 µH 20% 4.3A	COILCRAFT	MSS1278-683MLB
1	Q1	NMOS 100V 32A	VISHAY	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.2Ω 1% 1W	VISHAY	WSL2512R2000FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_{UVH}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

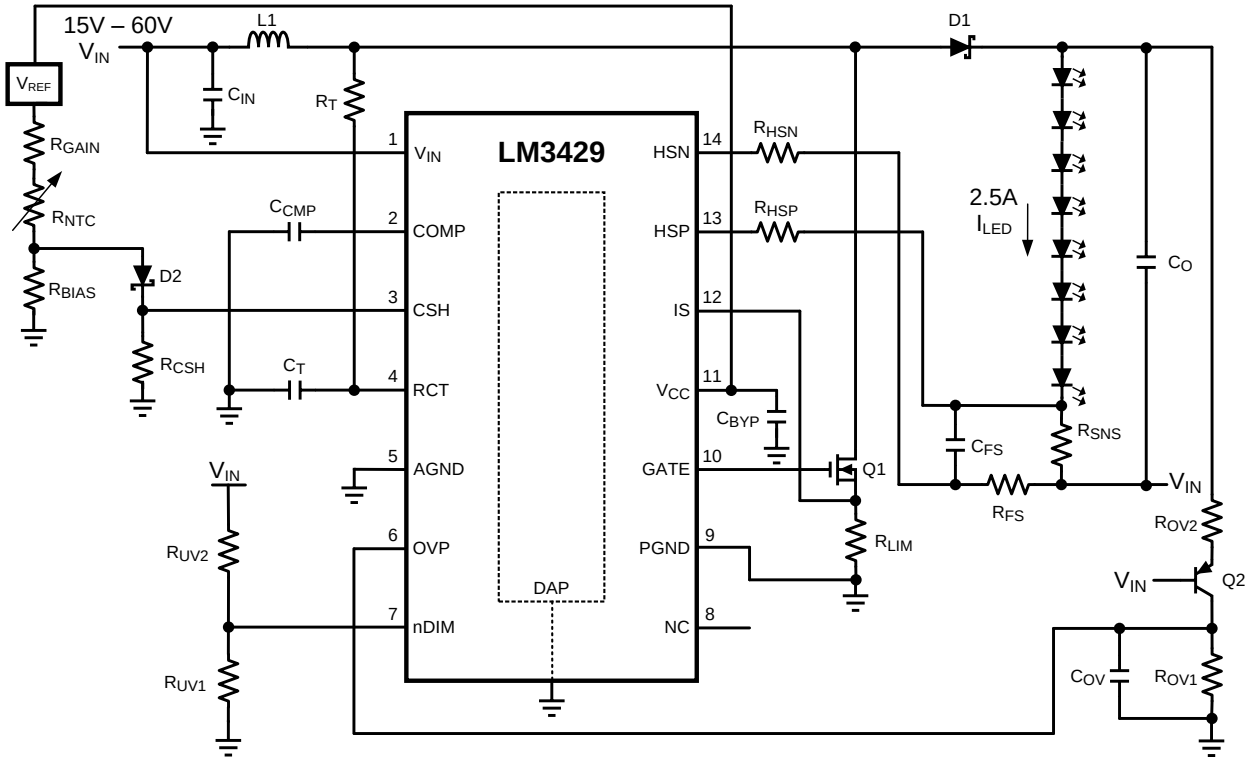
DESIGN #6: BUCK APPLICATION - 3 LEDS AT 1.25A



Design #6 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	0.015 µF X7R 10% 50V	MURATA	GRM21BR71H153KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.01 µF X7R 10% 50V	MURATA	GRM21BR71H103KA01L
2	C_{IN}	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_O	1 µF X7R 10% 50V	TDK	C4532X7R1H105K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	22 µH 20% 7.3A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	21.5 kΩ 1%	VISHAY	CRCW080521K5FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.08Ω 1% 1W	VISHAY	WSL2512R0800FEA
1	R_{UV1}	11.5 kΩ 1%	VISHAY	CRCW080511K5FKEA
1	R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA

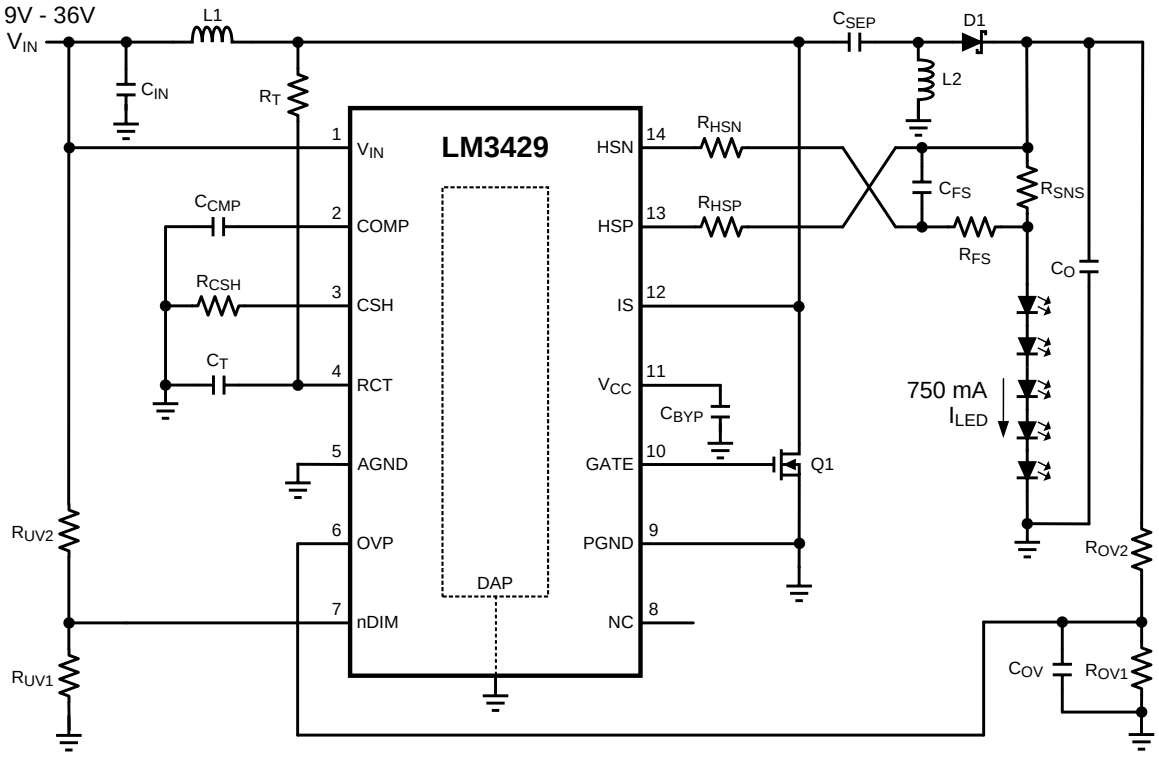
DESIGN #7: BUCK-BOOST THERMAL FOLDBACK APPLICATION - 8 LEDs at 2.5A



Design #7 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
3	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
1	C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	22 µH 20% 7.2A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
2	R_{LIM}, R_{SNS}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{UV1}	13.7 kΩ 1%	VISHAY	CRCW080513K7FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA

DESIGN #8: SEPIC APPLICATION - 5 LEDs at 750mA



Design #8 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3429	Boost controller	TI	LM3429MH
1	C_{CMP}	0.47 µF X7R 10% 25V	MURATA	GRM21BR71E474KA01L
1	C_F	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
2, 1	C_{IN}, C_O	6.8 µF X7R 10% 50V	TDK	C4532X7R1H685K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_{SEP}	1.0 µF X7R 10% 100V	TDK	C4532X7R2A105K
1	C_T	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1, L2	68 µH 20% 4.3A	COILCRAFT	DO3340P-683
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	NMOS 60V 115 mA	ON SEMI	2N7002ET1G
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	750Ω 1%	VISHAY	CRCW0805750RFKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
2	R_{OV1}, R_{UV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA

REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	44

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3429MH/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3429 MH	Samples
LM3429MHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3429 MH	Samples
LM3429Q1MH/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3429 Q1MH	Samples
LM3429Q1MHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3429 Q1MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LM3429, LM3429-Q1 :

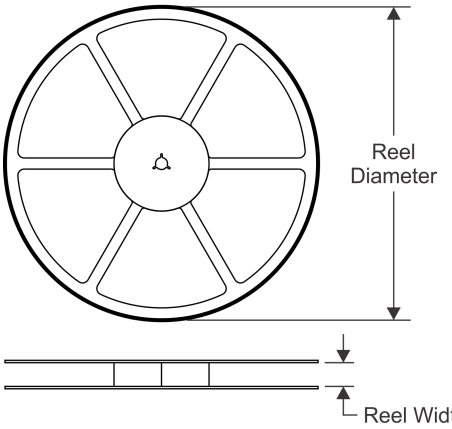
- Catalog: LM3429
- Automotive: LM3429-Q1

NOTE: Qualified Version Definitions:

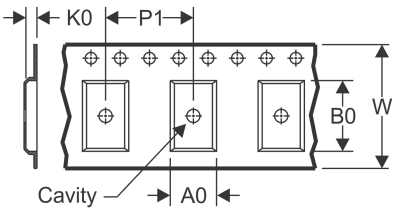
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

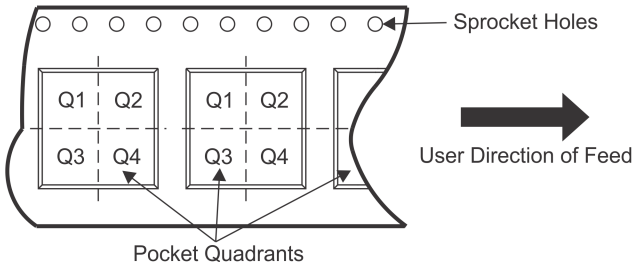


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

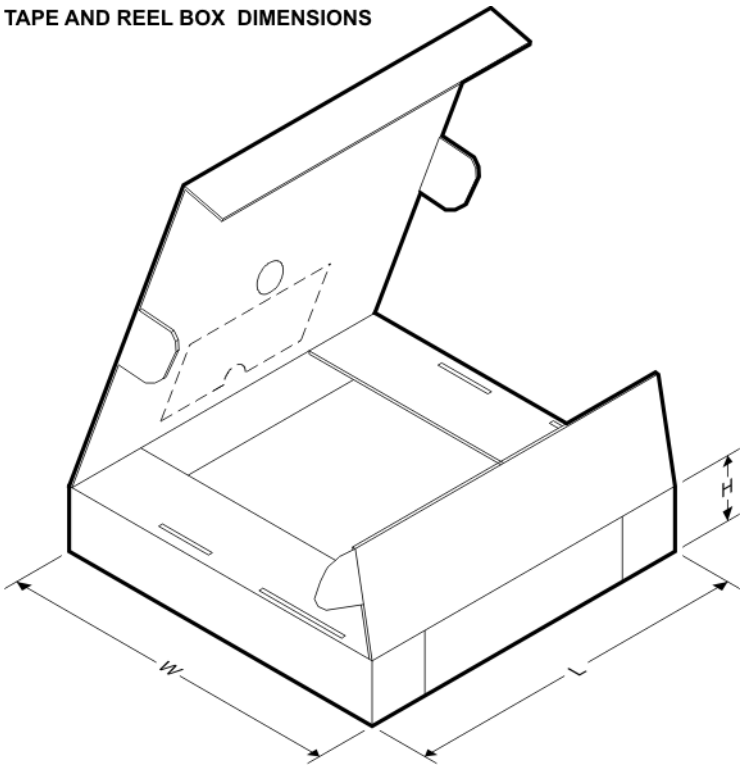
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3429MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM3429Q1MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

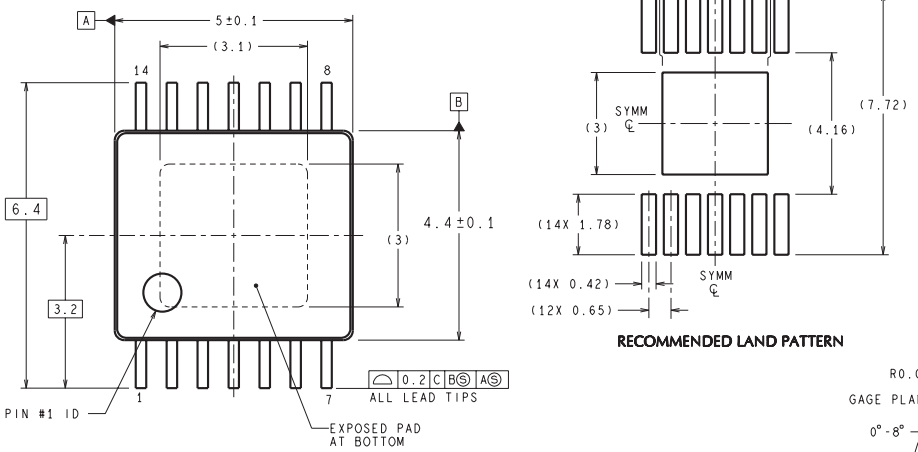
TAPE AND REEL BOX DIMENSIONS



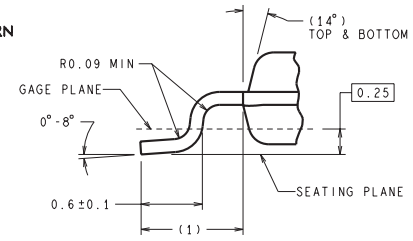
*All dimensions are nominal

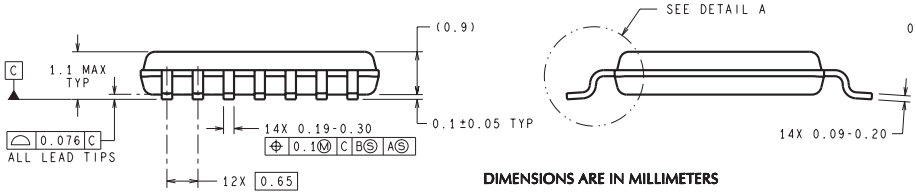
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3429MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM3429Q1MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0

PWP0014A



RECOMMENDED LAND PATTERN





DIMENSIONS ARE IN MILLIMETERS

MXA14A (Rev A)

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