



ISOLATED 5-V FULL AND HALF-DUPLEX RS-485 TRANSCEIVERS

 Check for Samples: [ISO3080](#), [ISO3086](#), [ISO3082](#), [ISO3088](#)

FEATURES

- **4000-V_{PEAK} Isolation, 560-V_{peak} V_{IORM}**
 - UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), IEC 61010-1, IEC 60950-1 and CSA Approved
- **Bus-Pin ESD Protection**
 - 12 kV HBM Between Bus Pins and GND2
 - 6 kV HBM Between Bus Pins and GND1
- **1/8 Unit Load – Up to 256 Nodes on a Bus**
- **Meets or Exceeds TIA/EIA RS-485 Requirements**
- **Signaling Rates up to 20 Mbps**
- **Thermal Shutdown Protection**
- **Low Bus Capacitance – 16 pF (Typ)**
- **50 kV/μs Typical Transient Immunity**
- **Fail-safe Receiver for Bus Open, Short, Idle**
- **3.3-V Inputs are 5-V Tolerant**

APPLICATIONS

- **Security Systems**
- **Chemical Production**
- **Factory Automation**
- **Motor/Motion Control**
- **HVAC and Building Automation Networks**
- **Networked Security Stations**

| | | |
|---------|-------------|----------|
| ISO3080 | Full-Duplex | 200 kbps |
| ISO3086 | Full-Duplex | 20 Mbps |
| ISO3082 | Half-Duplex | 200 kbps |
| ISO3088 | Half-Duplex | 20 Mbps |

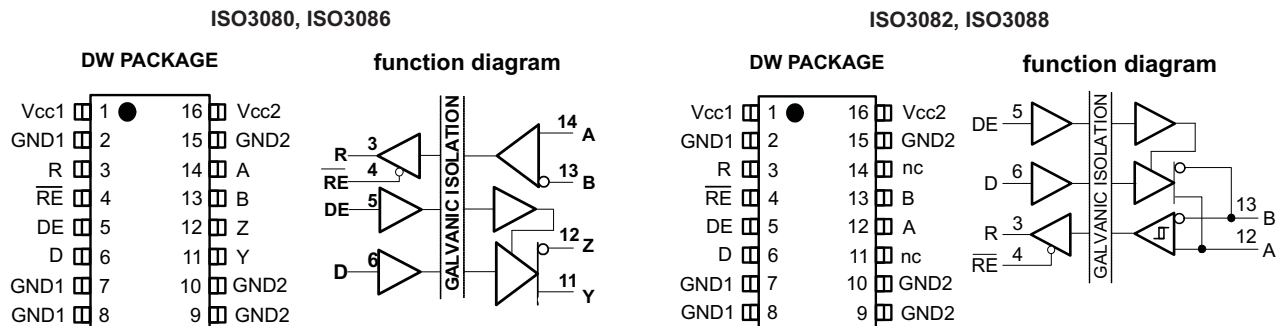
DESCRIPTION

The ISO3080, and ISO3086 are isolated full-duplex differential line drivers and receivers while the ISO3082, and ISO3088 are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications.

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 V_{rms} of isolation for 60s between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The ISO3080, ISO3082, ISO3086 and ISO3088 are qualified for use from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | | | VALUE | UNIT | |
|-----------|--|----------------------|--|-------------------|--------------------|----|
| V_{CC} | Input supply voltage, ⁽²⁾ V_{CC1} , V_{CC2} | | | -0.3 to 6 | V | |
| V_O | Voltage at any bus I/O terminal | | | -9 to 14 | V | |
| V_{IT} | Voltage input, transient pulse, A, B, Y, and Z (through 100 Ω , see Figure 11) | | | -50 to 50 | V | |
| V_I | Voltage input at any D, DE or \overline{RE} terminal | | | -0.5 to 7 | V | |
| I_O | Receiver output current | | | ± 10 | mA | |
| ESD | Electrostatic discharge | Human Body Model | JEDEC Standard 22, Test Method A114-C.01 | Bus pins and GND1 | ± 6 | kV |
| | | | | Bus pins and GND2 | ± 12 | |
| | | | | All pins | ± 4 | |
| | | Charged Device Model | JEDEC Standard 22, Test Method C101 | All pins | ± 1 | kV |
| | | Machine Model | ANSI/ESDS.5.2-1996 | | ± 200 | V |
| T_J | Maximum junction temperature | | | 150 | $^{\circ}\text{C}$ | |
| T_{STG} | Operating junction temperature | | | -65 to 150 | $^{\circ}\text{C}$ | |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

RECOMMENDED OPERATING CONDITIONS

| | | | | MIN | TYP | MAX | UNIT |
|-----------|--|--|------------------------|-------------------------------|-----|----------|--------------------|
| V_{CC1} | Logic-side supply voltage ⁽¹⁾ | | | 3.15 | | 5.5 | V |
| V_{CC2} | Bus-side supply voltage ⁽¹⁾ | | | 4.5 | 5 | 5.5 | V |
| V_{OC} | Voltage at either bus I/O terminal | | A, B | -7 | | 12 | V |
| V_{IH} | High-level input voltage | | D, DE, \overline{RE} | 2 | | V_{CC} | V |
| V_{IL} | Low-level input voltage | | | 0 | | 0.8 | |
| V_{ID} | Differential input voltage | | A with respect to B | -12 | | 12 | V |
| | | | Dynamic (ISO3086) | see Figure 14 | | | |
| R_L | Differential input resistance | | | 54 | 60 | | Ω |
| I_O | Output current | | Driver | -60 | | 60 | mA |
| | | | Receiver | -8 | | 8 | |
| T_J | Operating junction temperature | | | -40 | | 85 | $^{\circ}\text{C}$ |

- (1) For 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} is specified from 3.15 V to 3.6V.

SUPPLY CURRENT

over recommended operating condition (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|---------------------------|---|-------|-----|-----|------|
| I_{CC1} | Logic-side supply current | \overline{RE} at 0 V or V_{CC} , DE at 0 V or V_{CC1} | 3.3-V | | 8 | mA |
| | | \overline{RE} at 0 V or V_{CC} , DE at 0 V or V_{CC1} | 5-V | | 10 | |
| I_{CC2} | Bus-side supply current | \overline{RE} at 0 V or V_{CC} , DE at 0 V, No load | | | 15 | mA |

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|--|--|---|--------------------|-----|-----------------|-------|
| V _{OD} | Differential output voltage magnitude | I _O = 0 mA, no load | | 3 | 4.3 | V _{CC} | V |
| | | R _L = 54 Ω, See Figure 1 | | 1.5 | 2.3 | | |
| | | R _L = 100 Ω (RS-422), See Figure 1 | | 2 | 2.3 | | |
| | | V _{test} from –7 V to +12 V, See Figure 2 | | 1.5 | | | |
| Δ V _{OD} | Change in magnitude of the differential output voltage | See Figure 1 and Figure 2 | | –0.2 | 0 | 0.2 | V |
| V _{OC(SS)} | Steady-state common-mode output voltage | See Figure 3 | | 1 | 2.6 | 3 | V |
| ΔV _{OC(SS)} | Change in steady-state common-mode output voltage | | | –0.1 | | 0.1 | |
| V _{OC(pp)} | Peak-to-peak common-mode output voltage | See Figure 3 | | | 0.5 | | V |
| I _I | Input current | D, DE, V _I at 0 V or V _{CC1} | | –10 | | 10 | μA |
| I _{OZ} | High-impedance state output current | ISO3082 ISO3088 | See receiver input current | | | | μA |
| | | ISO3080 ISO3086 | V _Y or V _Z = 12 V, V _{CC} = 0 V or 5 V, DE = 0 V | Other input at 0 V | | | |
| V _Y or V _Z = –7 V, V _{CC} = 0 V or 5 V, DE = 0 V | | | –1 | | | | |
| I _{OS} | Short-circuit output current | V _A or V _B at –7 V | | –200 | | 200 | mA |
| | | V _A or V _B at 12 V | | | | | |
| CMTI | Common-mode transient immunity | See Figure 12 and Figure 13 | | 25 | 50 | | kV/μs |

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|---|-----------------|--------------------|---|-----|-----|------|
| t _{PLH} , t _{PHL} | Propagation delay | ISO3080/82 | | | 0.7 | 1.3 | μs |
| | | ISO3086/88 | | | 25 | 45 | |
| PWD ⁽¹⁾ | Pulse skew (t _{PHL} – t _{PLH}) | ISO3080/82 | | See Figure 4 | 20 | 200 | ns |
| | | ISO3086/88 | | | 3 | 7.5 | |
| t _r , t _f | Differential output signal rise and fall time | ISO3080/82 | | 0.5 | 0.9 | 1.5 | μs |
| | | ISO3086/88 | | 7 | 15 | | ns |
| t _{PZH} , t _{PZL} | Propagation delay, high-impedance-to-high-level output Propagation delay, high-impedance-to-low-level output | ISO3080/82 | 50% V _O | See Figure 5 and Figure 6 , DE at 0 V | 2.5 | 7 | μs |
| | | | 90% V _O | | 1.8 | | |
| t _{PHZ} , t _{PLZ} | Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output | ISO3086/88 | | 25 | 55 | ns | |
| | | ISO3080/82 | | 95 | 225 | | |
| | | ISO3086/88 | | 25 | 55 | | |

(1) Also known as pulse skew

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------|--|--|-----------------------|---------------|-------|------------|----|
| $V_{IT(+)}$ | Positive-going input threshold voltage | $I_O = -8$ mA | | -85 | -10 | mV | |
| $V_{IT(-)}$ | Negative-going input threshold voltage | $I_O = 8$ mA | -200 | -115 | | mV | |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | 30 | | mV | |
| V_{OH} | High-level output voltage | $V_{ID} = 200$ mV, $I_O = -8$ mA, See Figure 7 | 3.3-V V_{CC1} | $V_{CC1}-0.4$ | 3.1 | V | |
| | | | 5-V V_{CC1} | 4 | 4.8 | | |
| V_{OL} | Low-level output voltage | $V_{ID} = -200$ mV, $I_O = 8$ mA, See Figure 7 | 3.3-V V_{CC1} | | 0.15 | 0.4 | V |
| | | | 5-V V_{CC1} | | 0.15 | 0.4 | |
| $I_{O(Z)}$ | High-impedance state output current | $V_I = -7$ to 12 V, Other input = 0 V | | -1 | 1 | μ A | |
| I_I | Bus input current | V_A or $V_B = 12$ V | Other input at 0 V | | 0.04 | 0.1 | mA |
| | | V_A or $V_B = 12$ V, $V_{CC} = 0$ | | | 0.06 | 0.13 | |
| | | V_A or $V_B = -7$ V | | | -0.1 | -0.04 | |
| | | V_A or $V_B = -7$ V, $V_{CC} = 0$ | | | -0.05 | -0.03 | |
| I_{IH} | High-level input current, \overline{RE} | $V_{IH} = 2$ V | | -10 | 10 | μ A | |
| I_{IL} | Low-level input current, \overline{RE} | $V_{IL} = 0.8$ V | | -10 | 10 | μ A | |
| R_{ID} | Differential input resistance | A, B | | 48 | | k Ω | |
| C_D | Differential input capacitance | Test input signal is a 1.5 MHz sine wave with 1Vpp amplitude. CD is measured across A and B. | | 7 | | pF | |

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|--------------------------|-----|-----|-----|------|
| t_{PLH} , t_{PHL} | Propagation delay | See Figure 8 | | 90 | 125 | ns |
| PWD ⁽¹⁾ | Pulse width distortion [$t_{PHL} - t_{PLH}$] | | | 4 | 12 | |
| t_r , t_f | Output signal rise and fall time | | | 1 | | |
| t_{PHZ} , t_{PZH} | Propagation delay, high-level-to-high-impedance output Propagation delay, high-impedance-to-high-level output | See Figure 9, DE at 0 V | | | 22 | ns |
| t_{PZL} , t_{PLZ} | Propagation delay, high-impedance-to-low-level output Propagation delay, low-level-to-high-impedance output | See Figure 10, DE at 0 V | | | 22 | ns |

(1) Also known as pulse skew.

PARAMETER MEASUREMENT INFORMATION

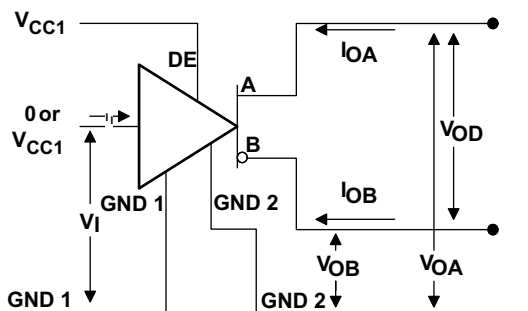


Figure 1. Driver V_{OD} Test and Current Definitions

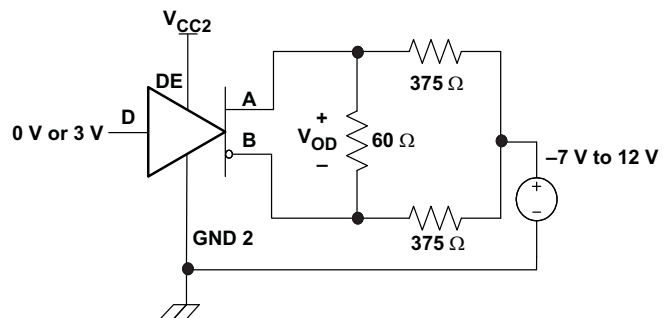


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

Note: Unless otherwise stated, test circuits are shown for half-duplex devices, ISO3082 & ISO3088. For full-duplex devices, driver output pins are Y and Z.

PARAMETER MEASUREMENT INFORMATION (continued)

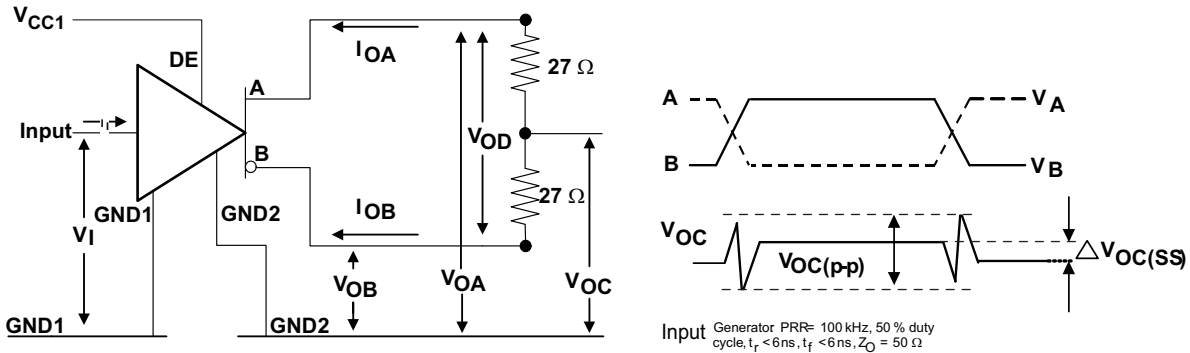


Figure 3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

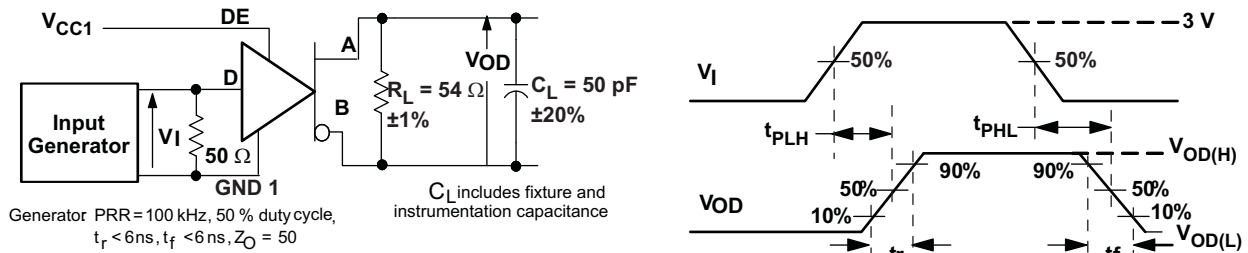


Figure 4. Driver Switching Test Circuit and Voltage Waveforms

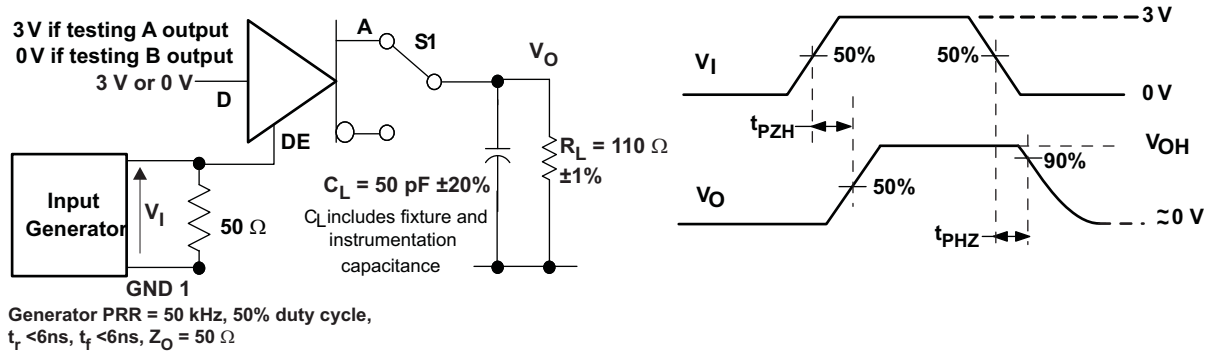


Figure 5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

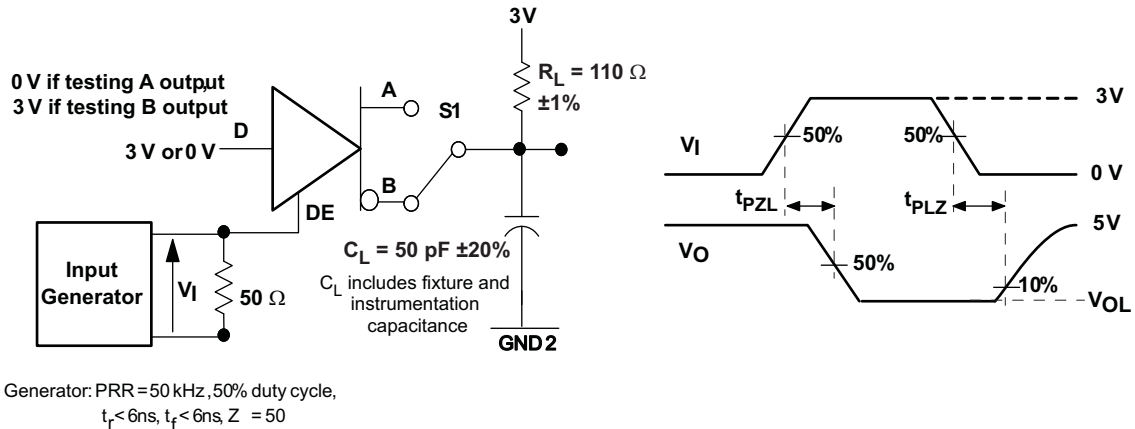


Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

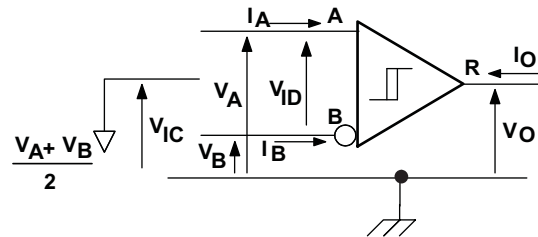


Figure 7. Receiver Voltage and Current Definitions

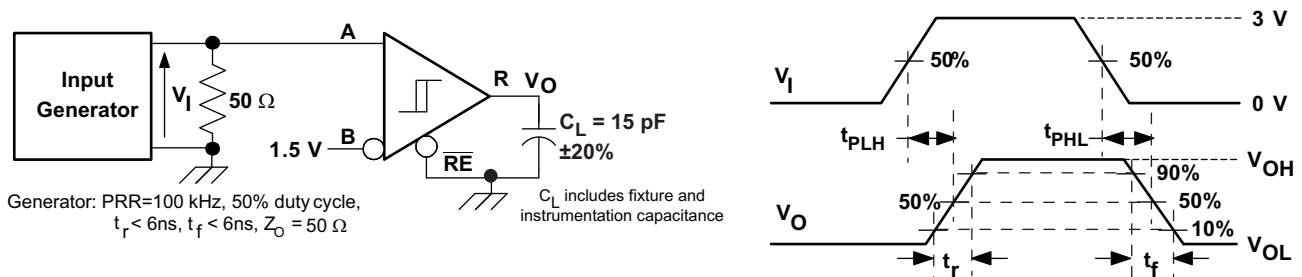


Figure 8. Receiver Switching Test Circuit and Waveforms

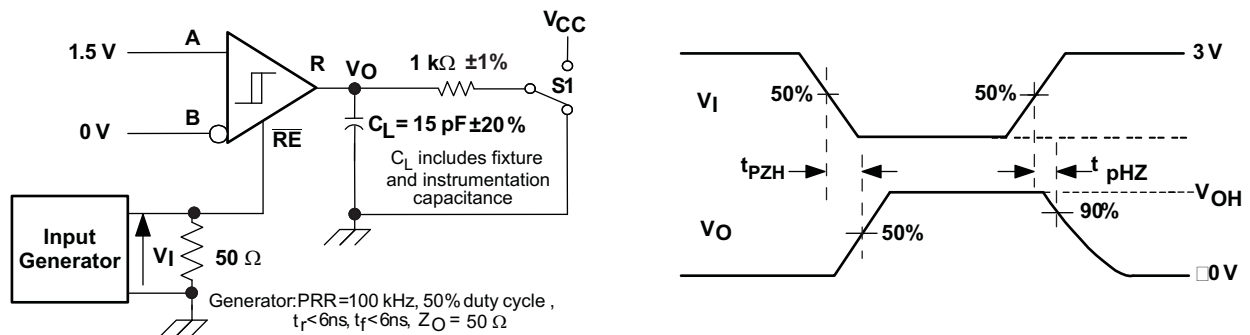


Figure 9. Receiver Enable Test Circuit and Waveforms, Data Output High

PARAMETER MEASUREMENT INFORMATION (continued)

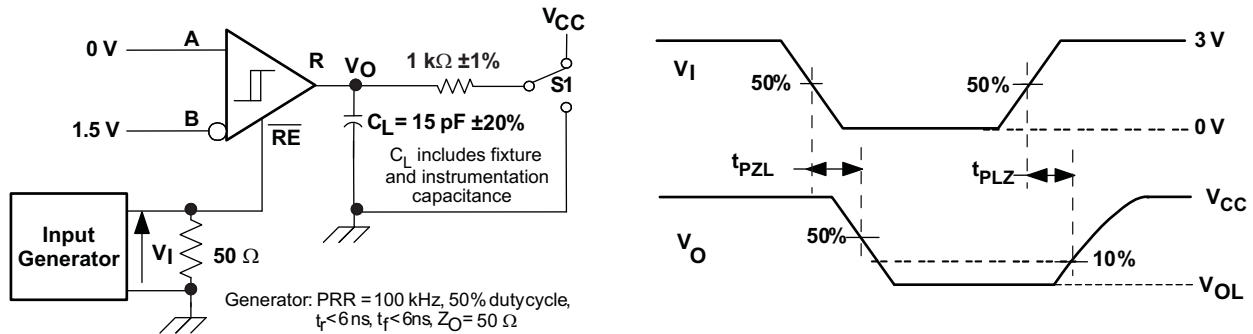
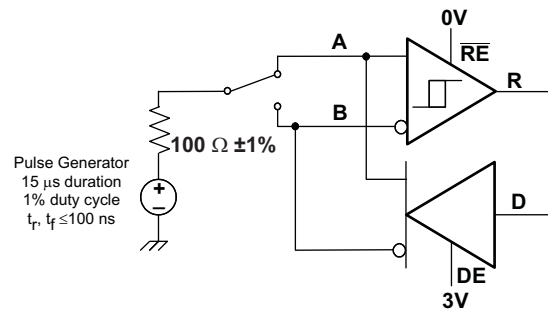


Figure 10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Transient Over-Voltage Test Circuit

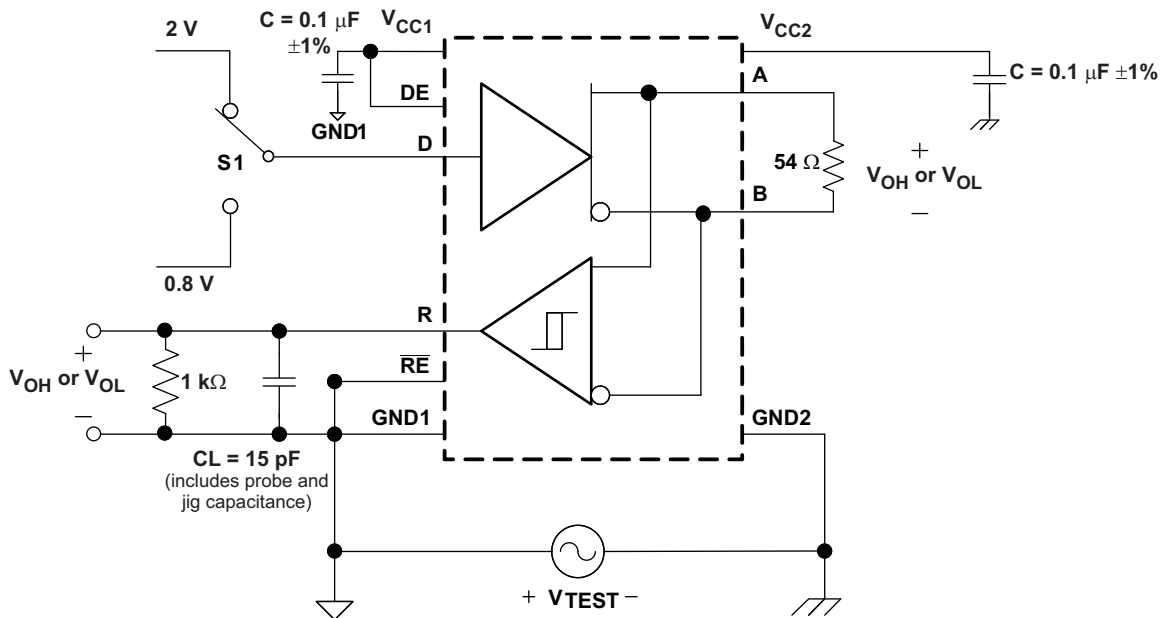


Figure 12. Half-Duplex Common-Mode Transient Immunity Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

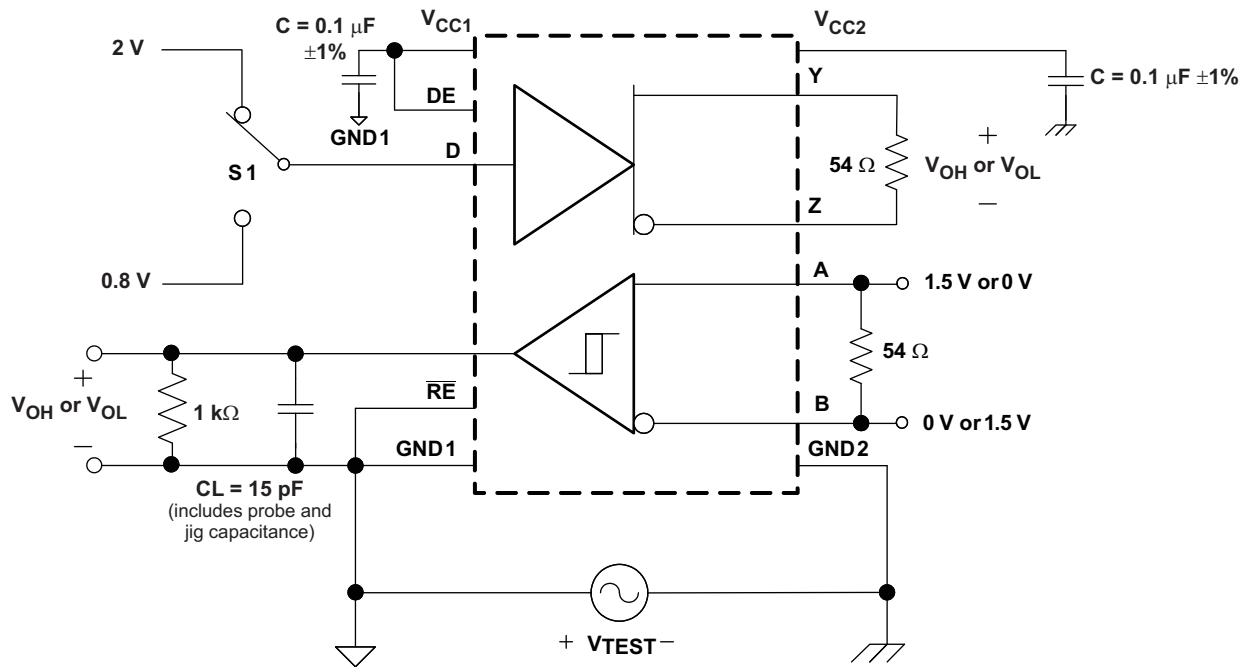


Figure 13. Full-Duplex Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

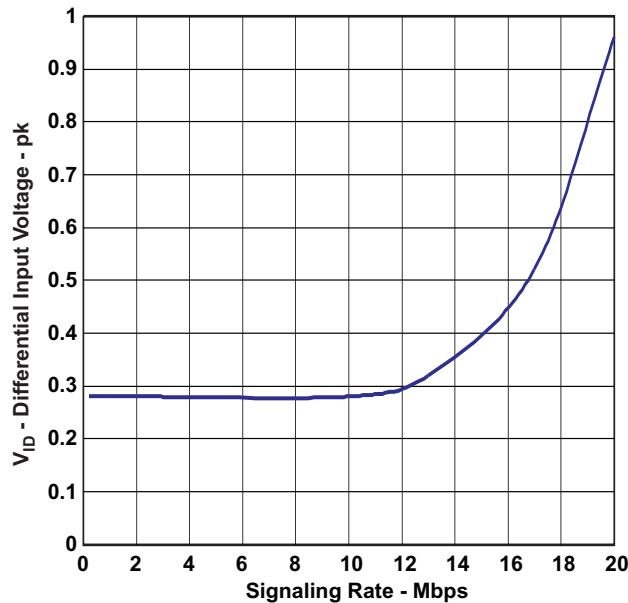


Figure 14. ISO3086 Recommended Minimum Differential Input Voltage vs Signaling Rate

Table 1. Driver Function Table⁽¹⁾

| V _{CC1} | V _{CC2} | INPUT (D) | ENABLE INPUT (DE) | OUTPUTS ⁽¹⁾ | |
|------------------|------------------|--------------|-------------------------|------------------------|-------|
| | | | | Y / A | Z / B |
| PU | PU | H | H | H | L |
| PU | PU | L | H | L | H |
| PU | PU | X | L | hi-Z | hi-Z |
| PU | PU | X | OPEN | hi-Z | hi-Z |
| PU | PU | OPEN | H | H | L |
| PD | PU | X | X | hi-Z | hi-Z |
| PU | PD | X | X | hi-Z | hi-Z |
| PD | PD | X | X | hi-Z | hi-Z |

(1) Driver output pins are Y & Z for full-duplex devices and A & B for half-duplex devices.

Table 2. Receiver Function Table⁽¹⁾

| V _{CC1} | V _{CC2} | DIFFERENTIAL INPUT V _{ID} = (V _A – V _B) | ENABLE (RE) | OUTPUT (R) |
|------------------|------------------|--|----------------|---------------|
| PU | PU | -0.01 V ≤ V _{ID} | L | H |
| PU | PU | -0.2 V < V _{ID} < -0.01 V | L | ? |
| PU | PU | V _{ID} ≤ -0.2 V | L | L |
| PU | PU | X | H | hi-Z |
| PU | PU | X | OPEN | hi-Z |
| PU | PU | Open circuit | L | H |
| PU | PU | Short Circuit | L | H |
| PU | PU | Idle (terminated) bus | L | H |
| PD | PU | X | X | hi-Z |
| PU | PD | X | L | H |

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, hi-Z = High Impedance (off), ? = Indeterminate

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|---|-------|-------------------|-----|------|
| L(I01) | Minimum air gap (Clearance) | Shortest terminal to terminal distance through air | 8.34 | | | mm |
| L(I02) | Minimum external tracking (Creepage) | Shortest terminal to terminal distance across the package surface | 8.1 | | | mm |
| CTI | Tracking resistance (Comparative Tracking Index) | DIN IEC 60112 / VDE 0303 Part 1 | ≥175 | | | V |
| | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| R _{IO} | Isolation resistance | Input to output, V _{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device | | >10 ¹² | | Ω |
| C _{IO} | Barrier capacitance Input to output | V _I = 0.4 sin (4E6πt) | | 2 | | pF |
| C _I | Input capacitance to ground | V _I = 0.4 sin (4E6πt) | | 2 | | pF |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|-----------------------------|--|---------------|
| Basic isolation group | Material group | IIIa |
| Installation classification | Rated mains voltage $\leq 150 V_{RMS}$ | I-IV |
| | Rated mains voltage $\leq 300 V_{RMS}$ | I-III |
| | Rated mains voltage $\leq 400 V_{RMS}$ | I-II |

IEC 60747-5-2 INSULATION CHARACTERISTICS ⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | UNIT |
|------------|------------------------------------|--|---------------|----------|
| V_{IORM} | Maximum working insulation voltage | | 560 | V |
| V_{PR} | Input to output test voltage | Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with $t = 1$ s, Partial discharge < 5 pC | 1050 | V |
| V_{IOTM} | Transient overvoltage | $t = 60$ s | 4000 | V |
| R_S | Insulation resistance | $V_{IO} = 500$ V at T_S | $>10^9$ | Ω |
| | Pollution degree | | 2 | |

(1) Climatic Classification 40/125/21

REGULATORY INFORMATION

| VDE | CSA | UL |
|--------------------------------------|--|--|
| Certified according to IEC 60747-5-2 | Approved under CSA Component Acceptance Notice | Recognized under 1577 Component Recognition Program ⁽¹⁾ |
| File Number: 40016131 | File Number: 220991 | File Number: E181974 |

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|-----------|---|-------|--|-----|-----|------------------|
| I_S | Safety input, output, or supply current | DW-16 | $\theta_{JA} = 168^\circ\text{C/W}$, $V_I = 5.5$ V, $T_J = 170^\circ\text{C}$, $T_A = 25^\circ\text{C}$ | | 157 | mA |
| T_S | Maximum case temperature | DW-16 | | | 150 | $^\circ\text{C}$ |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--------------------------------------|---|-----|------|-----|------|
| θ_{JA} | Junction-to-Air | Low-K Thermal Resistance ⁽¹⁾ | | 168 | | °C/W |
| | | High-K Thermal Resistance | | 96.1 | | |
| θ_{JB} | Junction-to-Board Thermal Resistance | | | 61 | | °C/W |
| θ_{JC} | Junction-to-Case Thermal Resistance | | | 48 | | °C/W |
| P_D | Device Power Dissipation | $V_{CC1} = V_{CC2} = 5.25\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, Input a 20 MHz 50% duty cycle square wave | | | 220 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

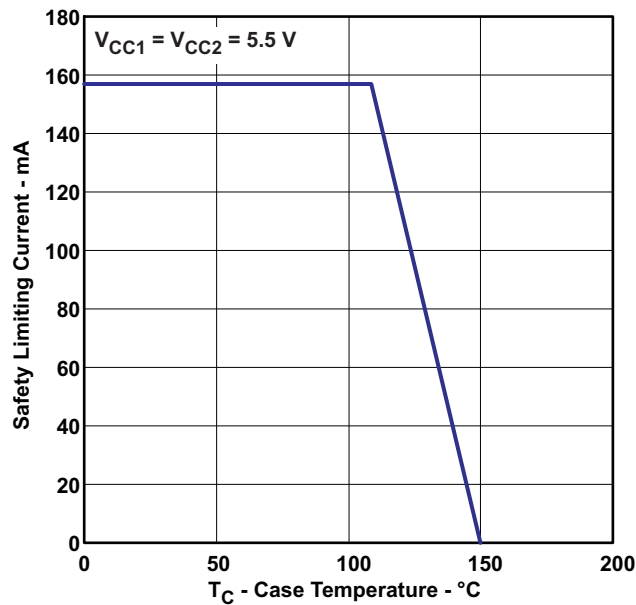
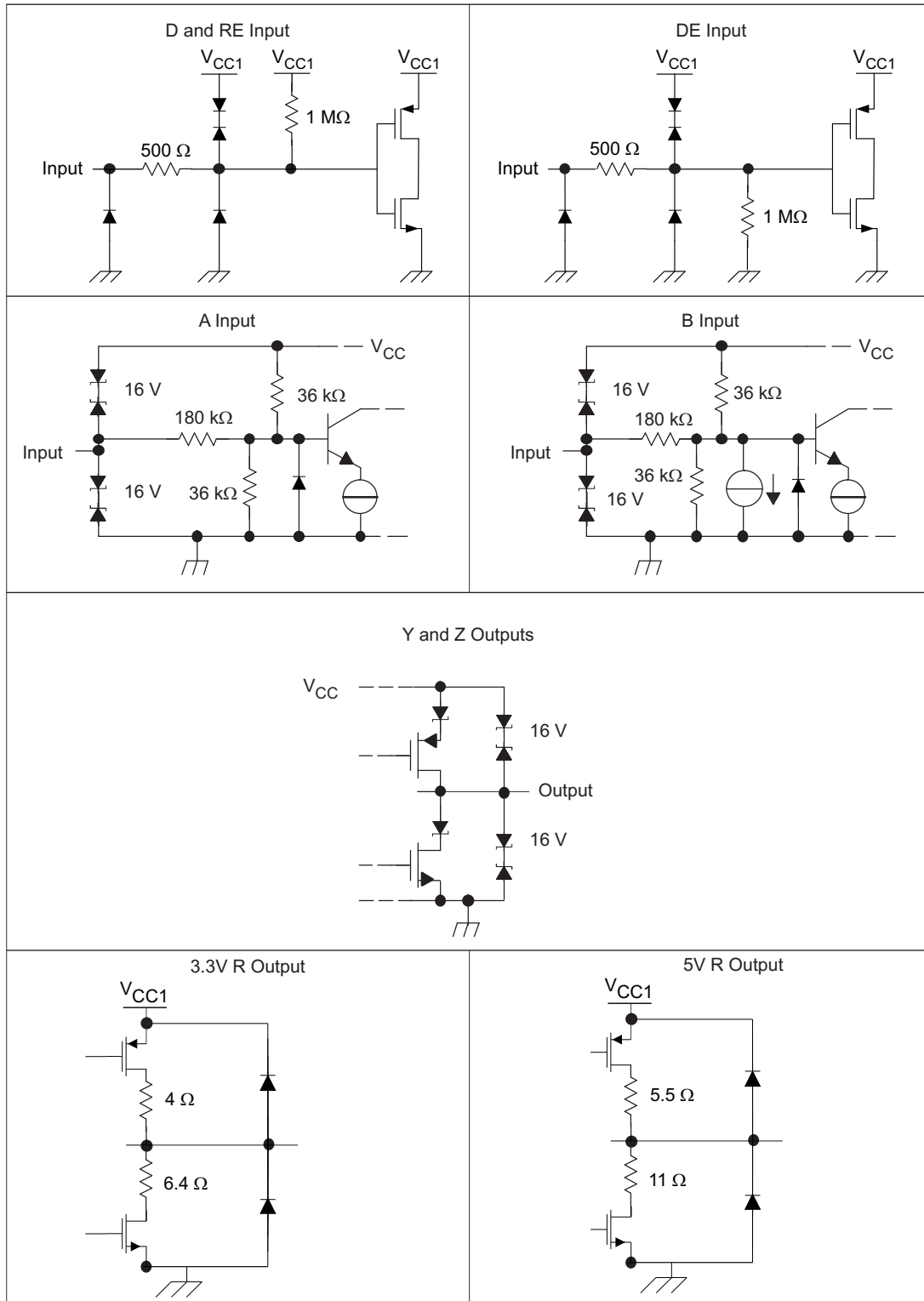


Figure 15. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

EQUIVALENT CIRCUIT SCHEMATICS



REVISION HISTORY

| Changes from Original (May 2008) to Revision A | Page |
|---|-------------|
| • Changed the Package Characteristics table - L(101) Minimum air gap (Clearance) From 7.7mm To 8.34mm | 9 |
| • Deleted the CSA column from the Regulatory Information Table. | 10 |
| • Changed the file number in the VDE column of the Regulatory Information table From: 40014131 To: 40016131 | 10 |
| Changes from Revision A (June 2008) to Revision B | Page |
| • Changed Features bullet From: 4000- V_{PEAK} Isolation, To: 4000- V_{PEAK} Isolation,, 560- V_{PEAK} V_{IORM} | 1 |
| • Added Features sub bullet: UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), IEC 61010-1, IEC 60950-1 and CSA Approved | 1 |
| • Added the CSA column to the Regulatory Information table | 10 |
| Changes from Revision B (December 2008) to Revision C | Page |
| • Changed Recommended Operatings Condition table note From: For 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6V. To: For 3-V operation, V_{CC1} is specified from 3.15 V to 3.6V. | 2 |
| Changes from Revision C (October 2009) to Revision D | Page |
| • Added T_{STG} row to the abs max table | 2 |
| • Added "Dynamic" conditions to Recommended Operating Conditions V_{ID} spec with reference to Figure 14 | 2 |
| • Changed for 3 V to 3.3 V in note 1 of the recommended operating table | 2 |
| • Deleted $V_I = V_{CCI}$ or 0 V from CMTI spec. Conditions statement. Added "Figure 13" | 3 |
| • Changed top row, UNIT column, split into 2 rows, top row μ s and second row ns | 3 |
| • Added note to bottom of first page of the Parameter Measurement information | 4 |
| • Added Figure 14 | 8 |
| • Added Footnotes to Driver Function Table and Receiver Function Table | 9 |
| • Changed File Number from '1698195' to '220991' in Regulatory Information table | 10 |
| • Changed θ_{JA} from 212°C/W to 168°C/W in conditions statement for I_S spec.; and MAX current from 210 mA to 157 mA | 10 |
| • Changed graph for "DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2", Figure 15 | 11 |
| Changes from Revision D (January 2011) to Revision E | Page |
| • Changed the second list item in FEATURES from 16 kV to 12 kV | 1 |
| • Changed ESD HBM spec in the ABS MAX TABLE, value from +/-16 to +/-12 | 2 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| ISO3080DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3080 | Samples |
| ISO3080DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3080 | Samples |
| ISO3080DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3080 | Samples |
| ISO3080DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3080 | Samples |
| ISO3082DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3082 | Samples |
| ISO3082DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3082 | Samples |
| ISO3082DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3082 | Samples |
| ISO3082DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3082 | Samples |
| ISO3086DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3086 | Samples |
| ISO3086DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3086 | Samples |
| ISO3086DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3086 | Samples |
| ISO3086DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3086 | Samples |
| ISO3088DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3088 | Samples |
| ISO3088DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3088 | Samples |
| ISO3088DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3088 | Samples |
| ISO3088DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ISO3088 | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO3080DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO3082DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO3086DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO3088DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO3080DWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO3082DWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO3086DWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO3088DWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R-PDSO-G16)

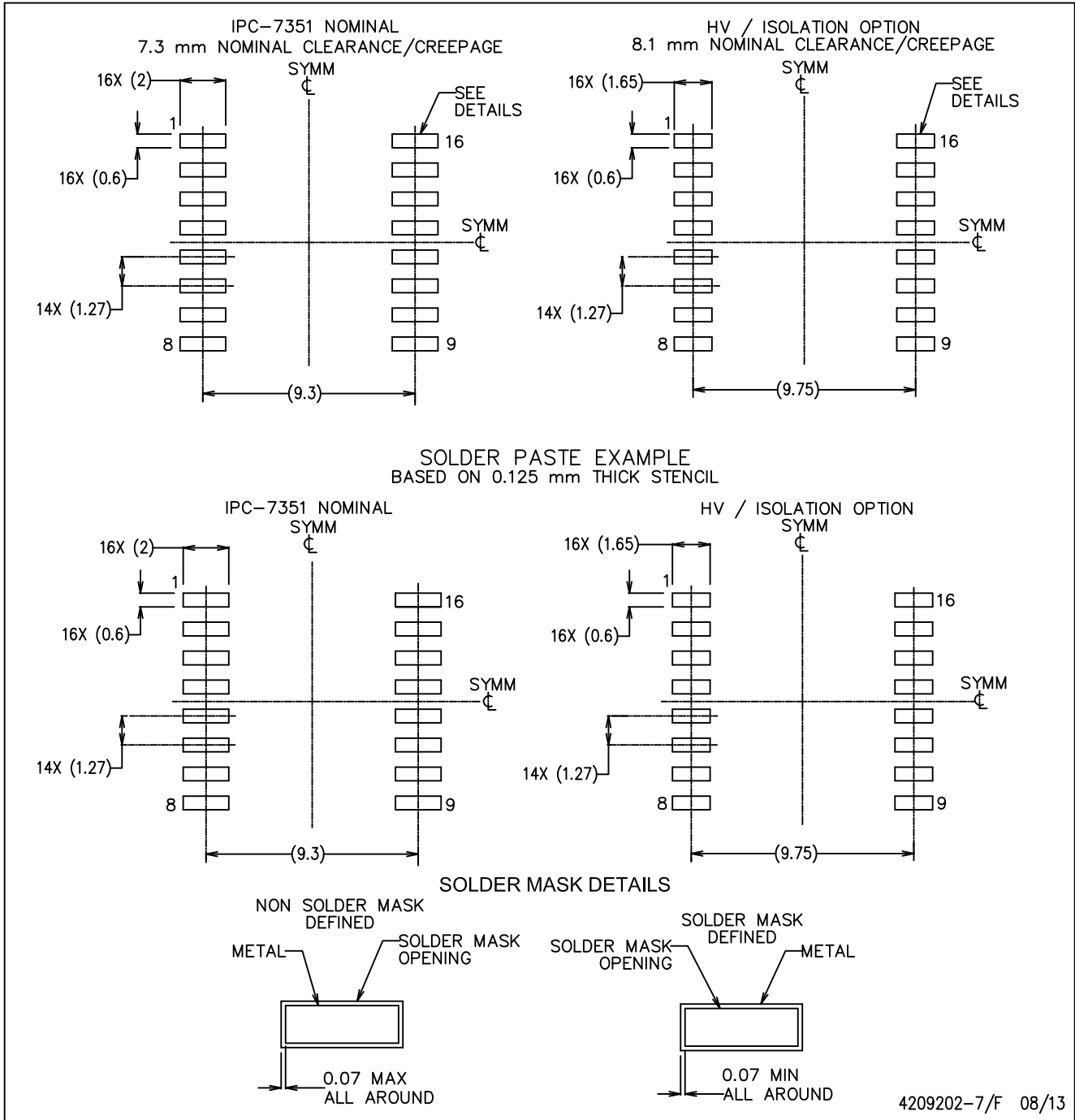
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
 - E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
 - F. Board assembly site may have different recommendations for stencil design.

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