+3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link–65 MHz, +3.3V LVDS Receiver 18-Bit Flat Panel Display (FPD) Link–65 MHz

Check for Samples: DS90C363, DS90CF364

FEATURES

- **20 to 65 MHz shift clock support**
- **Programmable Transmitter (DS90C363) strobe select (Rising or Falling edge strobe)**
- **Single 3.3V supply**
- **Chipset (TX + RX) power consumption < 250 mW (typ)**
- **Power-down mode (< 0.5 mW total)**
- **Single pixel per clock XGA (1024×768) ready**
- **Supports VGA, SVGA, XGA and higher addressability**
- **Up to 170 Megabyte/sec bandwidth**
- **Up to 1.3 Gbps throughput**
- **Narrow bus reduces cable size and cost**
- **290 mV swing LVDS devices for low EMI**
- **PLL requires no external components**
- **Low profile 48-lead TSSOP package**
- **Falling edge data strobe Receiver**
- **Compatible with TIA/EIA-644 LVDS standard**
- **ESD rating > 7 kV**
- **Operating Temperature: −40°C to +85°C**

DESCRIPTION

The DS90C363 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF364 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbyte/sec. The Transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The Transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge Transmitter will inter-operate with a Falling edge Receiver (DS90CF364) without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Block Diagrams

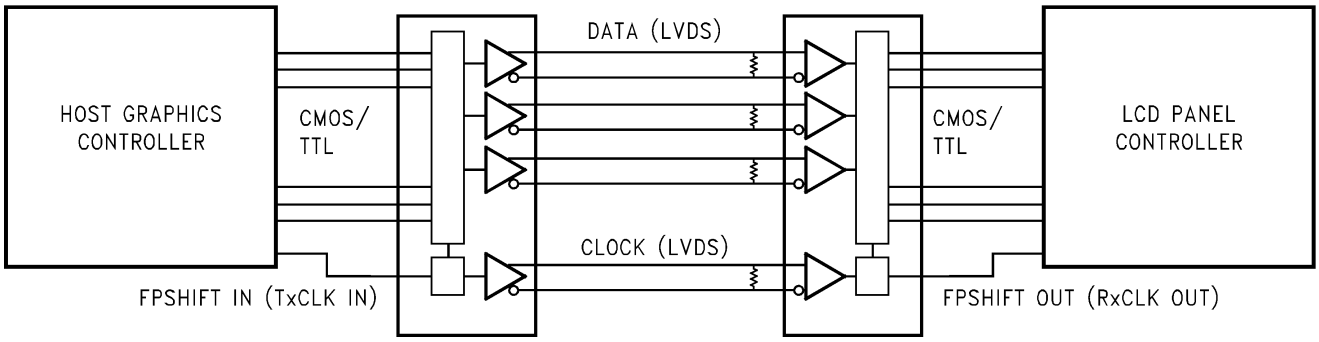


Figure 1. Application

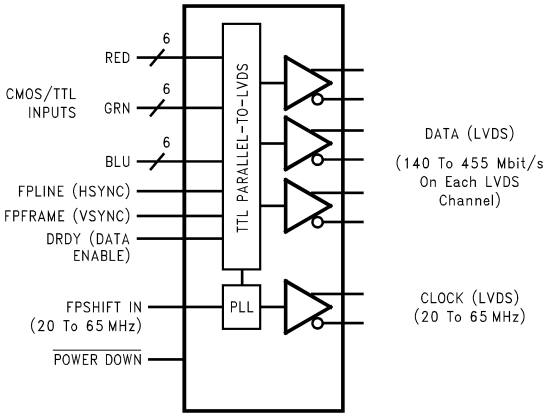


Figure 2. DS90C363

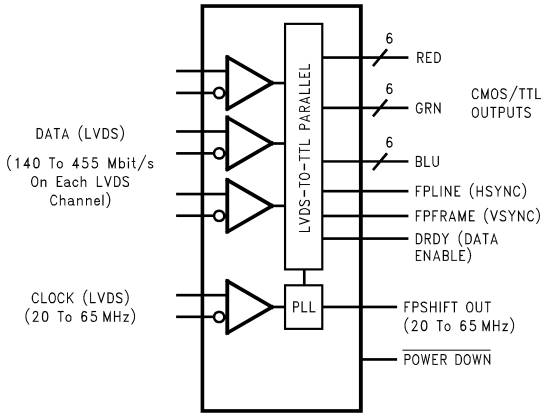


Figure 3. DS90CF364

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})		−0.3V to +4V
CMOS/TTL Input Voltage		−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration		Continuous
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		+260°C
Maximum Package Power Dissipation Capacity at 25°C (TSSOP Package)	DS90C363	1.98 W
	DS90CF364	1.89 W
Package Derating	DS90C363	16 mW/°C above +25°C
	DS90CF364	15 mW/°C above +25°C
ESD Rating	HBM, 1.5 kΩ, 100 pF	> 7 kV

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−60	−120	mA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (1)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{PWR\ DWN}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 4 Figure 6), T_A = −40°C to +85°C	f = 32.5 MHz		31	45	mA
			f = 37.5 MHz		32	50	mA
			f = 65 MHz		42	55	mA
ICCTG	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 5 Figure 6), T_A = −40°C to +85°C	f = 32.5 MHz		23	35	mA
			f = 37.5 MHz		28	40	mA
			f = 65 MHz		31	45	mA
ICCTZ	Transmitter Supply Current, Power Down	$\overline{PWR\ DWN}$ = Low, Driver Outputs in TRI-STATE® under Power Down Mode			10	55	µA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern (Figure 4 Figure 7), T_A = −40°C to +85°C	f = 32.5 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 65 MHz		78	105	mA
ICCRG	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern (Figure 5 Figure 7), T_A = −40°C to +85°C	f = 32.5 MHz		28	45	mA
			f = 37.5 MHz		30	47	mA
			f = 65 MHz		43	60	mA
ICCRZ	Receiver Supply Current, Power Down	$\overline{PWR\ DWN}$ = Low, Receiver Outputs Stay Low during Power Down Mode			10	55	µA

(1) V_{OS} previously referred as V_{CM}.

Transmitter Switching Characteristics

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
LLHT	LVDS Low-to-High Transition Time (Figure 6)			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 6)			0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 8)				5	ns
TCCS	TxOUT Channel-to-Channel Skew (Figure 9)			250		ps
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 20)	f = 65 MHz	−0.4	0	0.3	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.6	11.0	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period (Figure 10)		15	T	50	ns
TCIH	TxCLK IN High Time (Figure 10)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 10)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 10)	f = 65 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 10)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay at 25°C, V_{CC} = 3.3V (Figure 12)		3.0	3.7	5.5	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 14)				10	ms
TPDD	Transmitter Power Down Delay (Figure 18)				100	ns

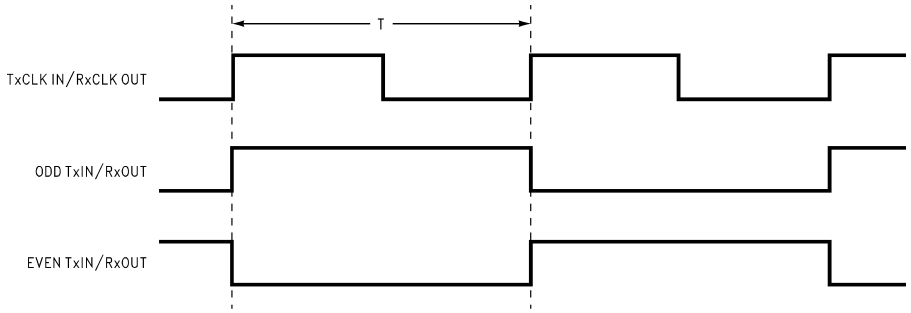
Receiver Switching Characteristics

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 7)			2.2	5.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 7)			2.2	5.0	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 21)	f = 65 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin (1) (Figure 22)	f = 65 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 11)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 11)	f = 65 MHz	7.3	8.6		ns
RCOL	RxCLK OUT Low Time (Figure 11)	f = 65 MHz	3.45	4.9		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 11)	f = 65 MHz	2.5	6.9		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 11)	f = 65 MHz	2.5	5.7		ns
RCCD	RxCLK IN to RxCLK OUT Delay at 25°C, V_{CC} = 3.3V (Figure 13)		5.0	7.1	9.0	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 15)				10	ms
RPDD	Receiver Power Down Delay (Figure 19)				1	µs

(1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

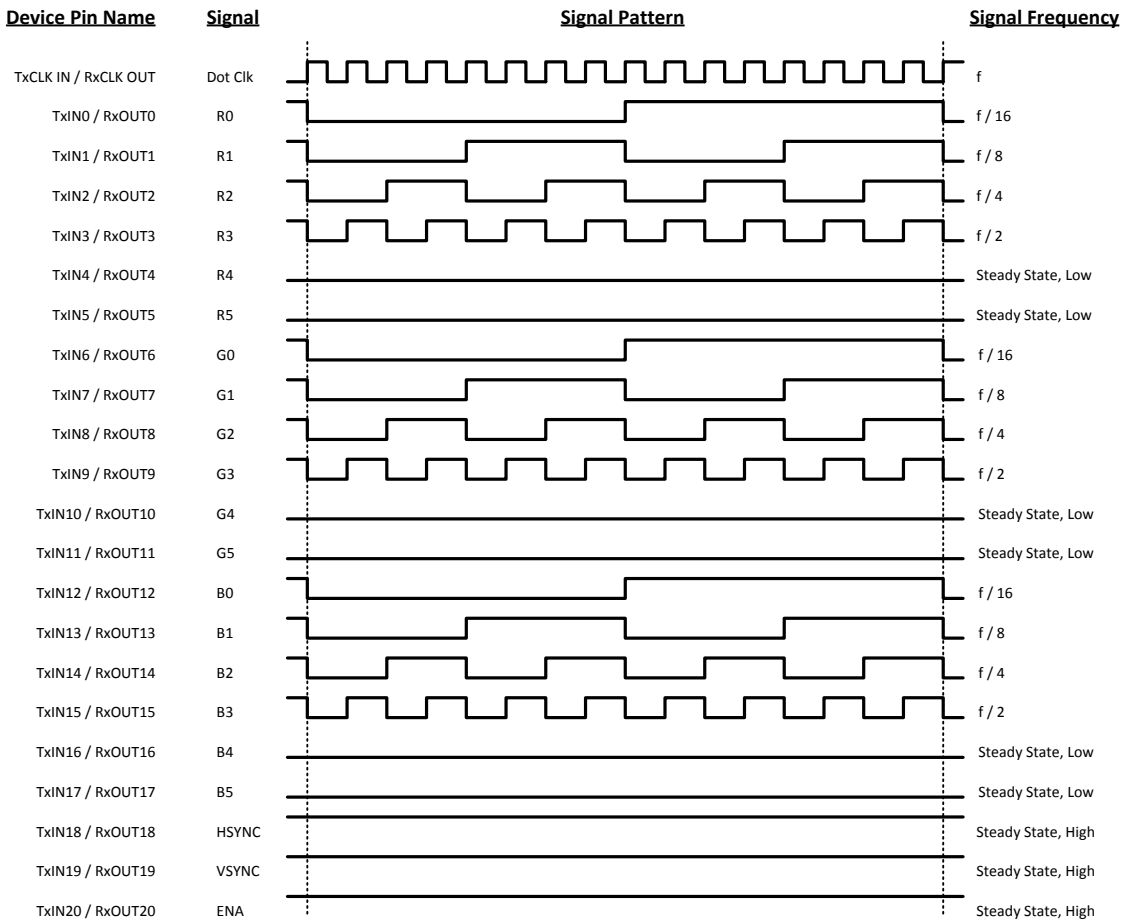
AC Timing Diagrams



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

B. Figure 4 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Figure 4. "Worst Case" Test Pattern



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

B. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

C. Figure 4 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

D. Recommended pin to signal mapping. Customer may choose to define differently.

Figure 5. "16 Grayscale" Test Pattern

AC Timing Diagrams (continued)

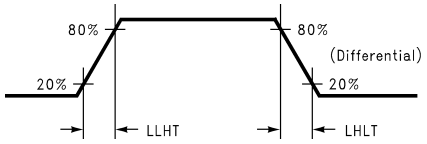


Figure 6. DS90C363 (Transmitter) LVDS Output Load and Transition Times

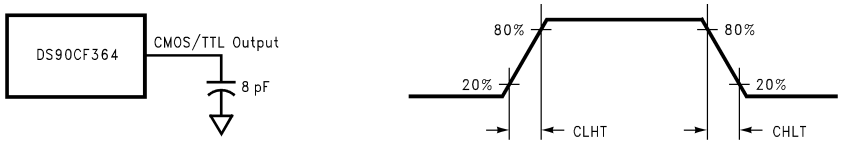


Figure 7. DS90CF364 (Receiver) CMOS/TTL Output Load and Transition Times

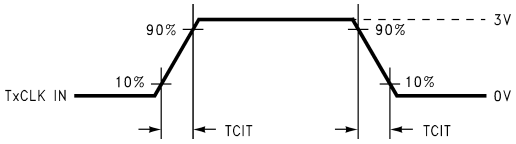
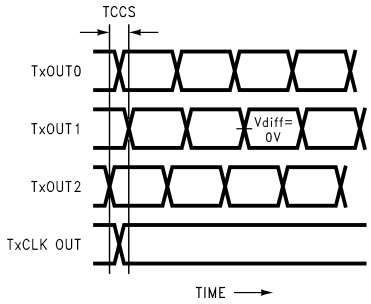


Figure 8. DS90C363 (Transmitter) Input Clock Transition Time



Measurements at Vdiff=0V
TCCS measured between earliest and latest LVDS edges
TxCLK Differential Low → High Edge

Figure 9. DS90C363 (Transmitter) Channel-to-Channel Skew

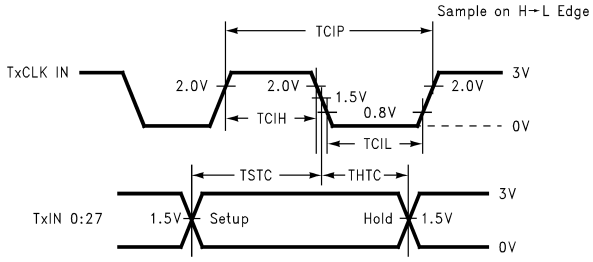


Figure 10. DS90C363 (Transmitter) Setup/Hold and High/Low Times

AC Timing Diagrams (continued)

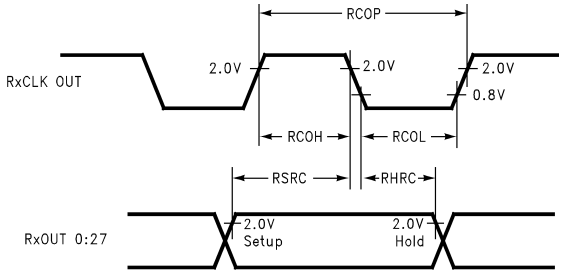


Figure 11. DS90CF364 (Receiver) Setup/Hold and High/Low Times

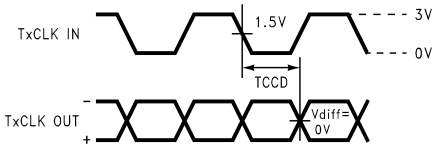


Figure 12. DS90C363 (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

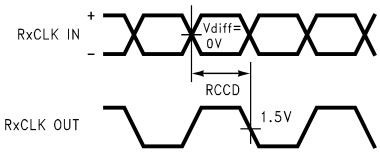


Figure 13. DS90CF364 (Receiver) Clock In to Clock Out Delay

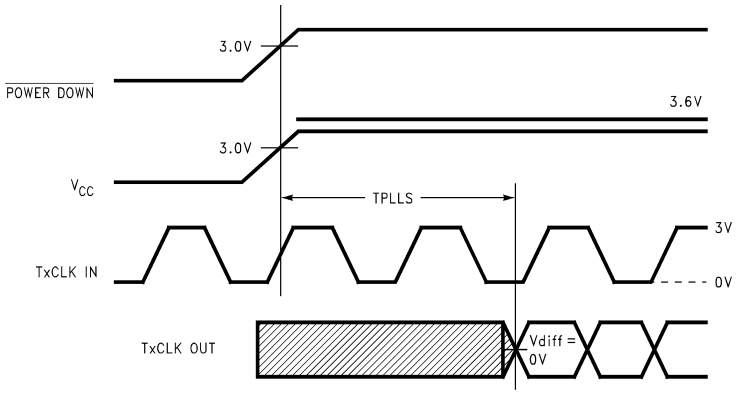


Figure 14. DS90C363 (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (continued)

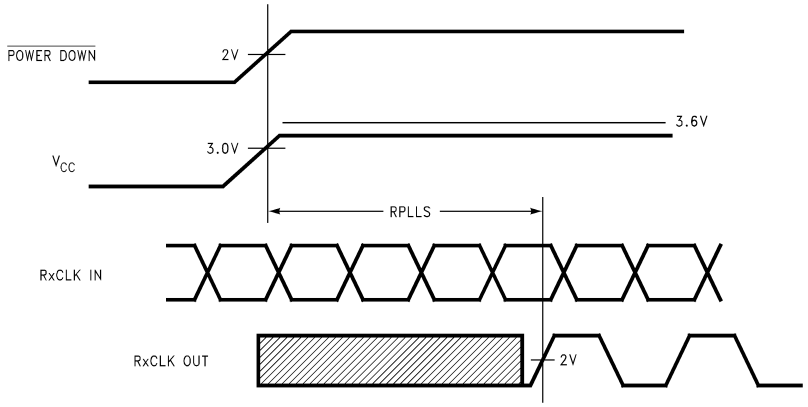


Figure 15. DS90CF364 (Receiver) Phase Lock Loop Set Time

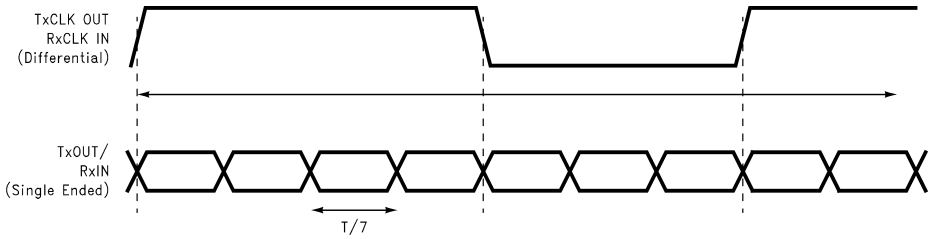


Figure 16. Seven Bits of LVDS in One Clock Cycle

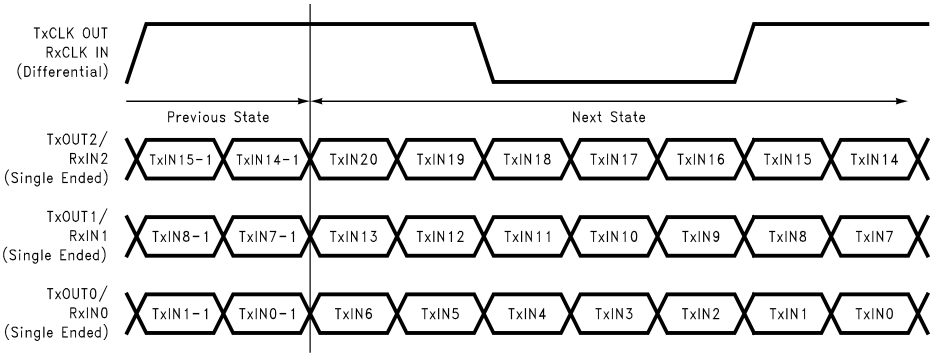


Figure 17. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

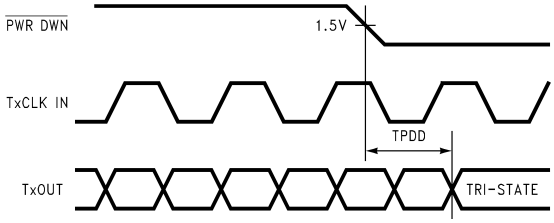


Figure 18. Transmitter Power Down Delay

AC Timing Diagrams (continued)

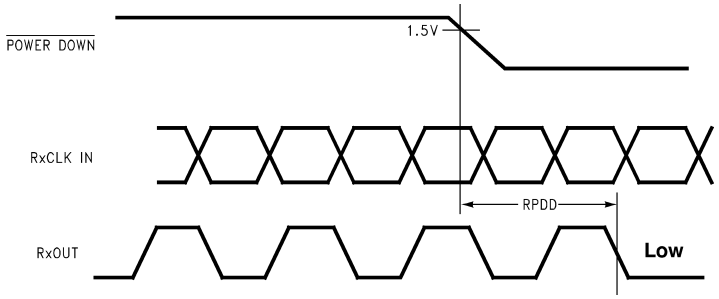


Figure 19. Receiver Power Down Delay

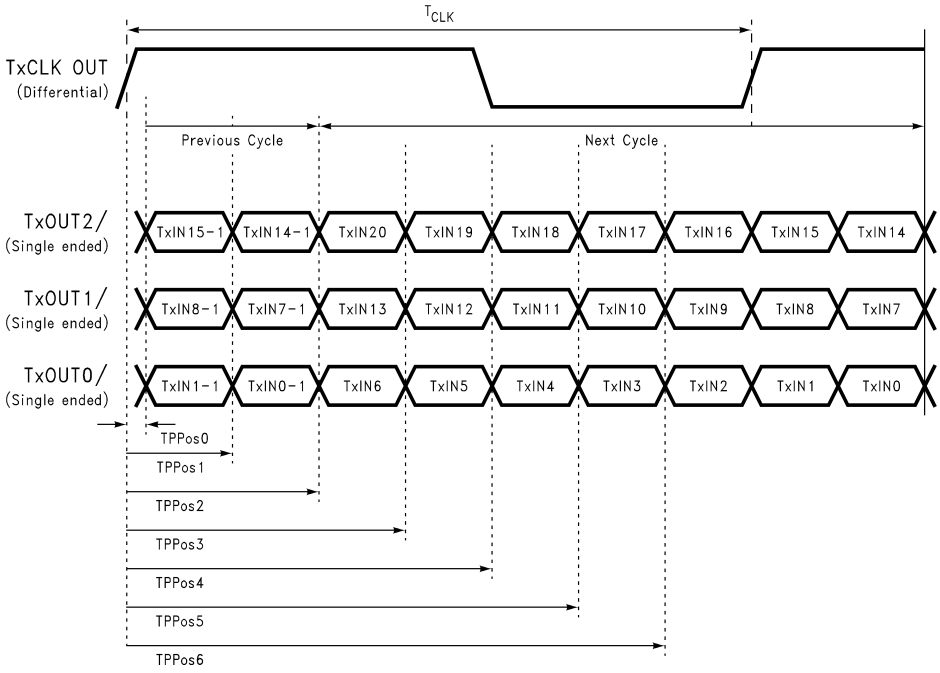


Figure 20. Transmitter LVDS Output Pulse Position Measurement

AC Timing Diagrams (continued)

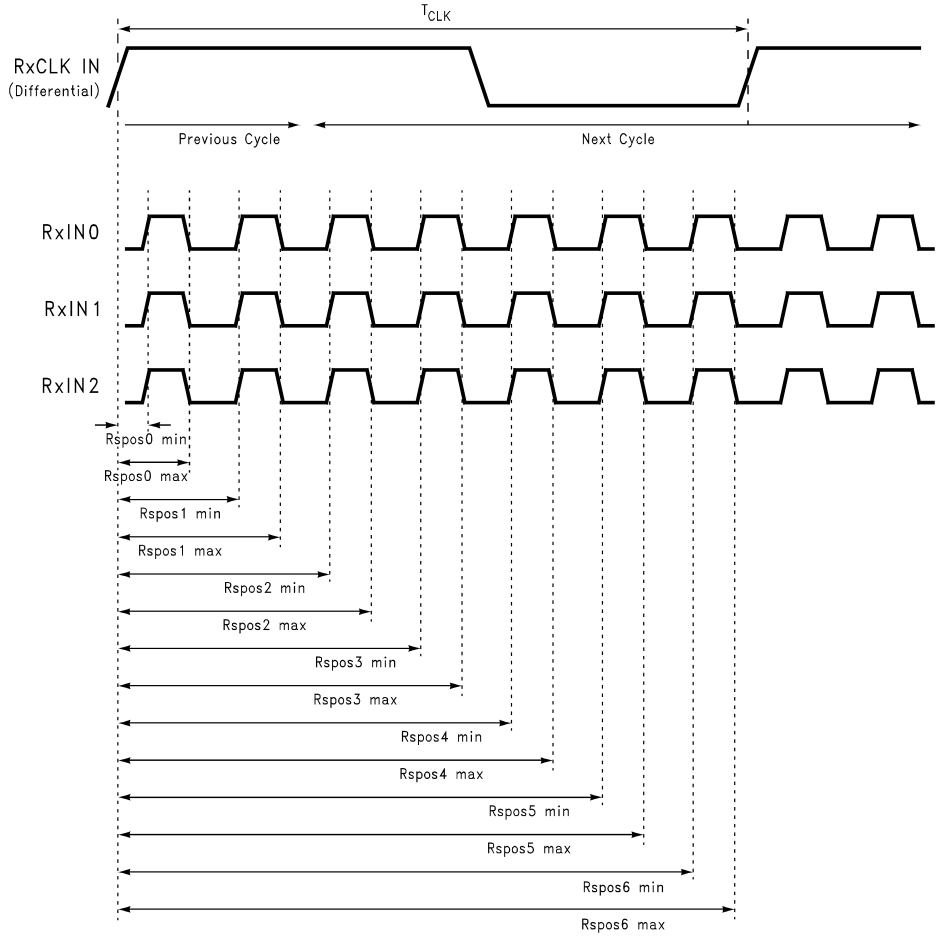
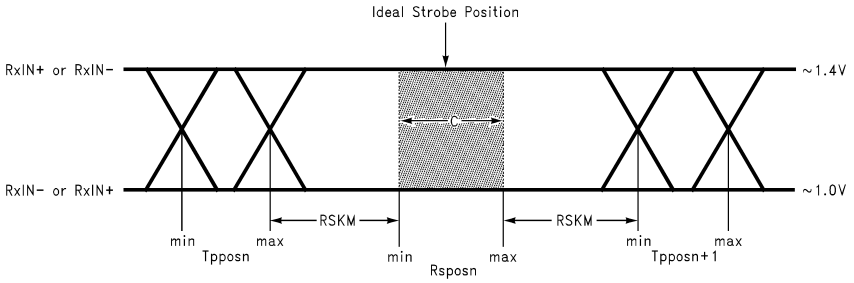


Figure 21. Receiver LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos—Transmitter output pulse position (min and max)
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
Cable Skew—typically 10 ps–40 ps per foot, media dependent

Cycle-to-cycle jitter is less than 250 ps at 65 MHz.

ISI is dependent on interconnect length; may be zero.

Figure 22. Receiver LVDS Input Skew Margin

PIN DESCRIPTIONS

DS90C363 Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select.
RTxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90CF364 Pin Descriptions — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.
RxIN−	I	3	Negative LVDS differential data inputs.
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Pin Diagrams

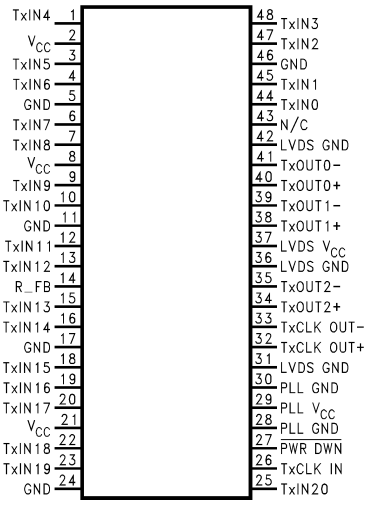


Figure 23. DS90C363
See Package Number DGG (R-PDSO-G48)

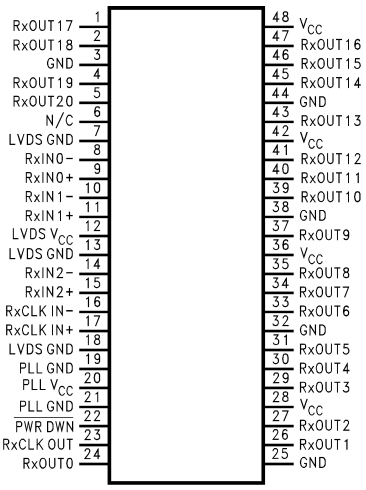


Figure 24. DS90CF364
See Package Number DGG (R-PDSO-G48)

Truth Table

Table 1. Programmable Transmitter

Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND	Falling edge strobe

APPLICATIONS INFORMATION

The DS90C363 and DS90CF364 are backward compatible with the existing 5V FPD Link transmitter/receiver pair (DS90CF563 and DS90CF564). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of both the transmitter and receiver devices. This change may enable the removal of a 5V supply from the system, and power may be supplied from an existing 3V power source.
2. The DS90C363 (transmitter) incorporates a rise/fall strobe select pin. This select function is on pin 14, formerly a V_{CC} connection on the 5V products. When the rise/fall strobe select pin is connected to V_{CC}, the part is configured with a rising edge strobe. In a system currently using a 5V rising edge strobe transmitter (DS90CR563), no layout changes are required to accommodate the new rise/fall select pin on the 3.3V transmitter. The V_{CC} signal may remain at pin 14, and the device will be configured with a rising edge strobe.
   – **When converting from a 5V falling edge transmitter (DS90CF563) to the 3V transmitter a minimal board layout change is necessary.** The 3.3V transmitter will not be configured with a falling edge strobe if V_{CC} remains connected to the select pin. To guarantee the 3.3V transmitter functions with a falling edge strobe pin 14 should be connected to ground OR left unconnected. When not connected (left open) and internal pull-down resistor ties pin 14 to ground, thus configuring the transmitter with a falling edge strobe.
3. The DS90C363 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90C363MTD	NRND	TSSOP	DGG	48	38	TBD	Call TI	Call TI		DS90C363MTD >B	
DS90C363MTD/NOPB	NRND	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		DS90C363MTD >B	
DS90C363MTDX/NOPB	NRND	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		DS90C363MTD >B	
DS90CF364MTD/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF364MTD >B	Samples
DS90CF364MTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF364MTD >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

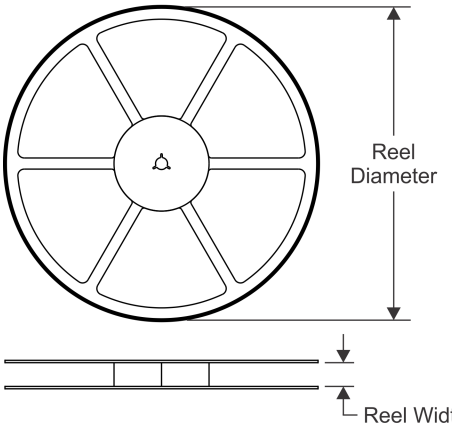
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

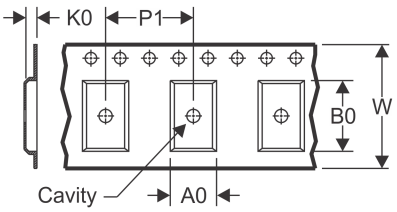
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

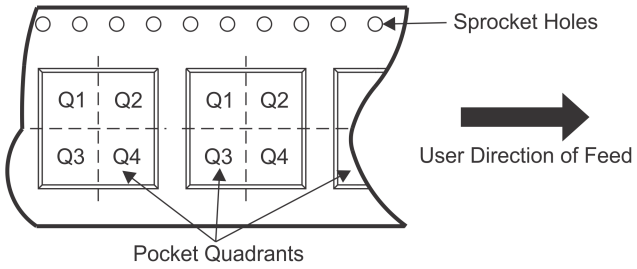


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

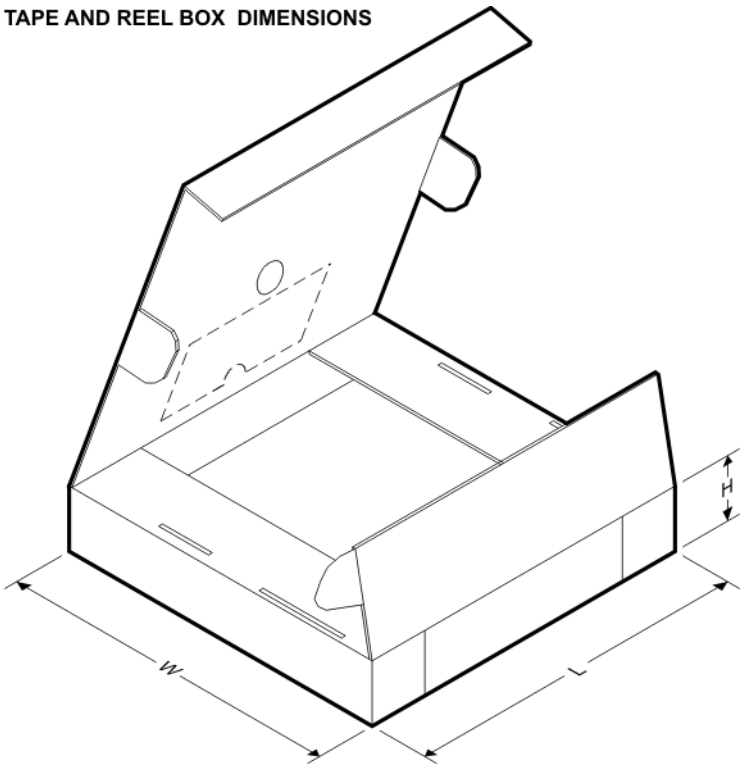
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C363MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CF364MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

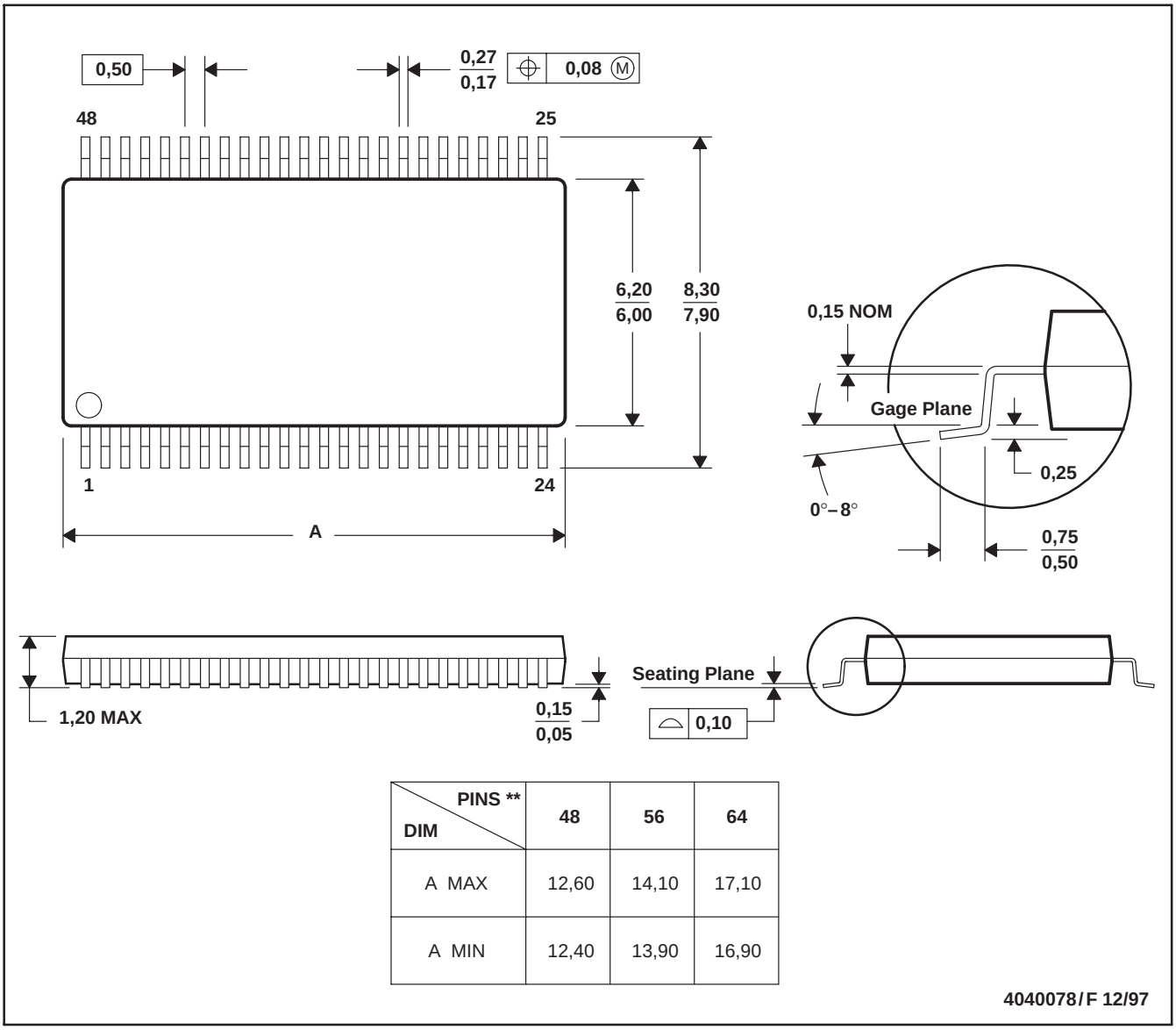


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C363MTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0
DS90CF364MTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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