# HIGH SPEED QUAD DIGITAL ISOLATORS

**Check for Samples: ISO7240CF, ISO7240C, ISO7240M, ISO7241C, ISO7241M, ISO7242C, ISO7242M**

## FEATURES

- **Selectable Failsafe Output (ISO7240CF)**
- **25 and 150-Mbps Signaling Rate Options**
  - **Low Channel-to-Channel Output Skew; 1 ns Max**
  - **Low Pulse-Width Distortion (PWD); 2 ns Max**
  - **Low Jitter Content; 1 ns Typ at 150 Mbps**
- **Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 18)**
- **4000-$V_{peak}$ $V_{IOTM}$, 560-$V_{peak}$ $V_{IORM}$ per IEC 60747-5-2 (VDE 0884, Rev 2)**
- **UL 1577 , IEC 61010-1, IEC 60950-1 and CSA Approved**
- **4 kV ESD Protection**
- **Operates With 2.8-V (ISO7241C), 3.3-V or 5-V Supplies**
- **High Electromagnetic Immunity (see application report SLLA181)**
- **–40°C to 125°C Operating Range**

## APPLICATIONS

- **Industrial Fieldbus**
- **Computer Peripheral Interface**
- **Servo Control Interface**
- **Data Acquisition**

## DESCRIPTION

The ISO7240, ISO7241 and ISO7242 are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide ($SiO_2$) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

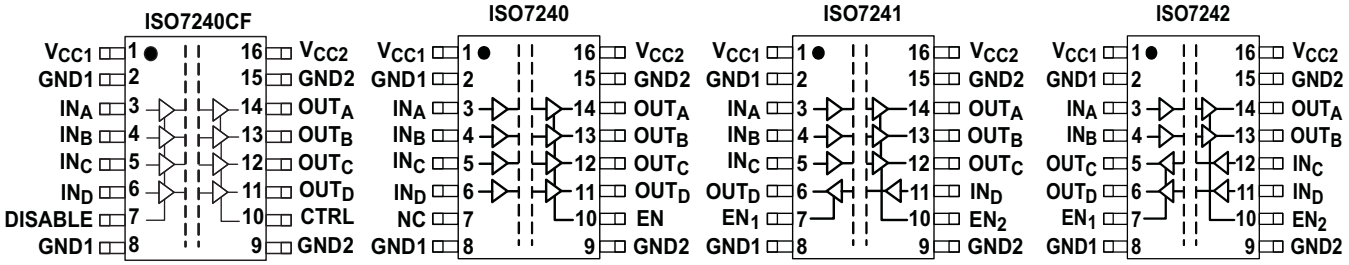
The ISO7240 has all four channels in the same direction while the ISO7241 has three channels the same direction and one channel in opposition. The ISO7242 has two channels in each direction.

The C option devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The M option devices have CMOS Vcc/2 input thresholds and do not have the input noise-filter or the additional propagation delay.

The ISO7240CF has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe-output is a logic high when a logic-high is placed on the CTRL pin or it is left unconnected. If a logic-low signal is applied to the CTRL pin, the failsafe-output becomes a logic-low output state. The ISO7240CF input disable function prevents data from being passed across the isolation barrier to the output. When the inputs are disabled, the outputs are set by the CTRL pin.

These devices may be powered from 2.8-V (ISO7241C only), 3.3-V or 5-V supplies on either side in any combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Table 1. Device Function Table ISO724x (1)**

| INPUT $V_{CC}$ | OUTPUT $V_{CC}$ | INPUT (IN) | OUTPUT ENABLE (EN) | OUTPUT (OUT) |
|---|---|---|---|---|
| PU | PU | H | H or Open | H |
| | | L | H or Open | L |
| | | X | L | Z |
| | | Open | H or Open | H |
| PD | PU | X | H or Open | H |
| PD | PU | X | L | Z |

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

**Table 2. ISO7240CF Function Table**

| $V_{CC1}$ | $V_{CC2}$ | DATA INPUT (IN) | DISABLE INPUT (DISABLE) | FAILSAFE CONTROL INPUT (CTRL) | DATA OUTPUT (OUT) |
|---|---|---|---|---|---|
| PU | PU | H | L or Open | X | H |
| PU | PU | L | L or Open | X | L |
| X | PU | X | H | H or Open | H |
| X | PU | X | H | L | L |
| PD | PU | X | X | H or Open | H |
| PD | PU | X | X | L | L |

**AVAILABLE OPTIONS**

| PRODUCT | SIGNALING RATE | INPUT THRESHOLD | CHANNEL CONFIGURATION | MARKED AS | ORDERING NUMBER(1) |
|---|---|---|---|---|---|
| ISO7240C | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | 4/0 | ISO7240C | ISO7240CDW (rail) |
| | | | | | ISO7240CDWR (reel) |
| ISO7240CF | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | | ISO7240CF | ISO7240CFDW (rail) |
| | | | | | ISO7240CFDWR (reel) |
| ISO7240M | 150 Mbps | Vcc/2 (CMOS) | | ISO7240M | ISO7240MDW (rail) |
| | | | | | ISO7240MDWR (reel) |
| ISO7241C | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | 3/1 | ISO7241C | ISO7241CDW (rail) |
| | | | | | ISO7241CDWR (reel) |
| ISO7241M | 150 Mbps | Vcc/2 (CMOS) | | ISO7241M | ISO7241MDW (rail) |
| | | | | | ISO7241MDWR (reel) |
| ISO7242C | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | 2/2 | ISO7242C | ISO7242CDW (rail) |
| | | | | | ISO7242CDWR (reel) |
| ISO7242M | 150 Mbps | Vcc/2 (CMOS) | | ISO7242M | ISO7242MDW (rail) |
| | | | | | ISO7242MDWR (reel) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

| | | | | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(2), $V_{CC1}$, $V_{CC2}$ | | | | –0.5 to 6 | V |
| $V_I$ | Voltage at IN, OUT, EN, DISABLE, CTRL | | | | –0.5 to 6 | V |
| $I_O$ | Output current | | | | ±15 | mA |
| ESD | Electrostatic discharge | Human Body Model | JEDEC Standard 22, Test Method A114-C.01 | All pins | ±4 | kV |
| | | Field-Induced-Charged Device Model | JEDEC Standard 22, Test Method C101 | | ±1 | |
| | | Machine Model | ANSI/ESDS5.2-1996 | | ±200 | V |
| $T_J$ | Maximum junction temperature | | | | 170 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(1), $V_{CC1}$, $V_{CC2}$ | ISO7240C/CF, ISO7242C, ISO724xM, | 3.15 | | 5.5 | V |
| | | ISO7241C | 2.8 | | 5.5 | |
| $I_{OH}$ | High-level output current | | -4 | | | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | mA |
| $t_{ui}$ | Input pulse width | ISO724xC | 40 | | | ns |
| | | ISO724xM | 6.67 | 5 | | |
| $1/t_{ui}$ | Signaling rate | ISO724xC | 0 | 30(2) | 25 | Mbps |
| | | ISO724xM | 0 | 200(2) | 150 | |
| $V_{IH}$ | High-level input voltage (IN) | ISO724xM | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (IN) | | 0 | | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage (IN, DISABLE, CTRL, EN) | ISO724xC | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (IN, DISABLE, CTRL, EN) | | 0 | | 0.8 | V |
| $T_J$ | Junction temperature | | | | 150 | °C |
| H | External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification | | | | 1000 | A/m |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.
For the 2.8-V operation (ISO7241C-only), $V_{CC1}$ or $V_{CC2}$ is specified at 2.8 V.
(2) Typical value at room temperature and well-regulated power supply.

## IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SPECIFICATIONS | UNIT |
|---|---|---|---|---|
| $V_{IORM}$ | Maximum working insulation voltage | | 560 | V |
| $V_{PR}$ | Input to output test voltage | After Input/Output Safety Test Subgroup 2/3<br>$V_{PR} = V_{IORM} \times 1.2$, t = 10 s,<br>Partial discharge < 5 pC | 672 | V |
| | | Method a, $V_{PR} = V_{IORM} \times 1.6$,<br>Type and sample test with t = 10 s,<br>Partial discharge < 5 pC | 896 | V |
| | | Method b1, $V_{PR} = V_{IORM} \times 1.875$,<br>100 % Production test with t = 1 s,<br>Partial discharge < 5 pC | 1050 | V |
| $V_{IOTM}$ | Transient overvoltage | t = 60 s | 4000 | V |
| $R_S$ | Insulation resistance | $V_{IO}$ = 500 V at $T_S$ | $>10^9$ | Ω |
| | Pollution degree | | 2 | |

(1) Climatic Classification 40/125/21

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V[(1)] OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 1 | 3 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 7 | 10.5 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V- | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6.5 | 11 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 12 | 18 | |
| | ISO7242C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 15 | 24 | |
| $I_{CC2}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V- | All channels, no load, EN at 3 V | | 15 | 22 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 17 | 25 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 13 | 20 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 18 | 28 | |
| | ISO7242C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 15 | 24 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | EN at 0 V, Single channel | | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA, See Figure 1 | | | $V_{CC}$–0.8 | | | V |
| | | $I_{OH}$ = –20 µA, See Figure 1 | | | $V_{CC}$–0.1 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, See Figure 1 | | | | | 0.4 | V |
| | | $I_{OL}$ = 20 µA, See Figure 1 | | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | IN from 0 V to $V_{CC}$ | | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, See Figure 5 | | | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 18 | | 42 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | See Figure 1 | | | 2.5 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 10 | | 23 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xC | | | | 8 | ns |
| | | ISO724xM | | | 0 | 3 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xC | | | | 2 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 12 | | µs |
| $t_{wake}$ | Wake time from input disable | | See Figure 4 | | 15 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 6 | | 1 | | ns |

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 1 | 3 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 7 | 10.5 | |
| | ISO7241C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6.5 | 11 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 12 | 18 | |
| | ISO7242C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 15 | 24 | |
| $I_{CC2}$ | ISO7240C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 9.5 | 15 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 10.5 | 17 | |
| | ISO7241C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 8 | 13 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 11.5 | 18 | |
| | ISO7242C/M | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 9 | 14 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | EN at 0 V, Single channel | | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA, See Figure 1 | | ISO7240 | $V_{CC}$–0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$–0.8 | | | |
| | | $I_{OH}$ = –20 µA, See Figure 1 | | | $V_{CC}$–0.1 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, See Figure 1 | | | | | 0.4 | V |
| | | $I_{OL}$ = 20 µA, See Figure 1 | | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | IN from 0 V to $V_{CC}$ | | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See Figure 5 | | | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 20 | | 50 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | | | | 3 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | | 12 | | 29 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xC | | | | 10 | ns |
| | | ISO724xM | | | 0 | 5 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xC | | | | 3 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 18 | | µs |
| $t_{wake}$ | Wake time from input disable | | See Figure 4 | | 15 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 6 | | 1 | | ns |

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 0.5 | 1 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 3 | 5 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 4 | 7 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 6.5 | 11 | |
| | ISO724C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 9 | 14 | |
| $I_{CC2}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 15 | 22 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 17 | 25 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 13 | 20 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 18 | 28 | |
| | ISO7242C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 15 | 24 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | EN at 0 V, Single channel | | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA, See Figure 1 | | ISO7240 | $V_{CC}$ – 0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$ – 0.8 | | | |
| | | $I_{OH}$ = –20 µA, See Figure 1 | | | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, See Figure 1 | | | | | 0.4 | V |
| | | $I_{OL}$ = 20 µA, See Figure 1 | | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | IN from 0 V to $V_{CC}$ | | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, See Figure 5 | | | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 22 | | 51 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | See Figure 1 | | | 3 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 12 | | 30 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xC | | | | 10 | ns |
| | | ISO724xM | | | 0 | 5 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xC | | | | 2.5 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 12 | | µs |
| $t_{wake}$ | Wake time from input disable | | See Figure 4 | | 15 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 6 | | 1 | | ns |

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3 V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 0.5 | 1 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 3 | 5 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 4 | 7 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 6.5 | 11 | |
| | ISO7242C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 9 | 14 | |
| $I_{CC2}$ | ISO7240C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, EN at 3 V | | 9.5 | 15 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 10.5 | 17 | |
| | ISO7241C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 8 | 13 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 11.5 | 18 | |
| | ISO7242C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 9 | 14 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | EN at 0 V, single channel | | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA, See Figure 1 | | | $V_{CC}$–0.4 | | | V |
| | | $I_{OH}$ = –20 µA, See Figure 1 | | | $V_{CC}$–0.1 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, See Figure 1 | | | | | 0.4 | V |
| | | $I_{OL}$ = 20 µA, See Figure 1 | | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | IN from 0 V or $V_{CC}$ | | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, See Figure 5 | | | 25 | 50 | | kV/µs |

(1) For the 3.3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 25 | | 56 | ns |
| PWD | Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1) | ISO724xC | See Figure 1 | | | 4 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 12 | | 34 | ns |
| PWD | Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1) | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xC | | | | 10 | ns |
| | | ISO724xM | | | 0 | 5 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xC | | | | 3.5 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 18 | | µs |
| $t_{wake}$ | Wake time from input disable | | See Figure 4 | | 15 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 6 | | 1 | | ns |

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 2.8 V (ISO7241C only)(1) OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7241C | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 3.9 | 6.8 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 6.2 | 10.5 | |
| $I_{CC2}$ | ISO7241C | Quiescent | $V_I = V_{CC}$ or 0 V | All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6.9 | 12 | mA |
| | | 25 Mbps | 12.5 MHz Input Clock Signal | | | 9.4 | 16 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | $EN_1$ at 0 V, single channel | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | | $V_{CC}$–0.6 | | | V |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | | $V_{CC}$–0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | | 0.6 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V or $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | 2 | | pF |
| CMTI | Common-mode transient immunity | | $V_I = V_{CC}$ or 0 V, See Figure 5 | | 10 | 45 | | kV/µs |

(1) For the 2.8-V operation, $V_{CC1}$ or $V_{CC2}$ is specified at 2.8-V.
2.8-V operation is only guaranteed for ISO7241C with production screening starting in January 2012. The first two digits of the Lot Trace Code (YMLLLLS) written on top of each device can be used to identify year and month of production respectively.

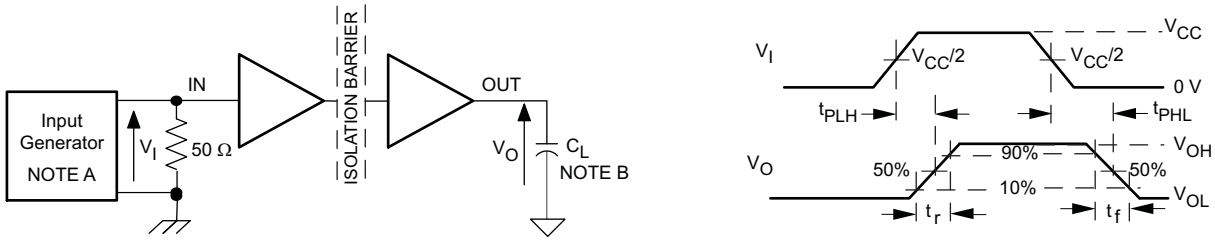
## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 2.8-V OPERATION (ISO7241C only)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO7241C | See Figure 1 | 25 | | 70 | ns |
| PWD | Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1) | ISO7241C | See Figure 1 | | | 5 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO7241C | | | | 12 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO7241C | | | | 5 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 25 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 25 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 25 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 25 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 7 | | µs |
| $t_{wake}$ | Wake time from input disable | | See Figure 4 | | 12 | | µs |

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

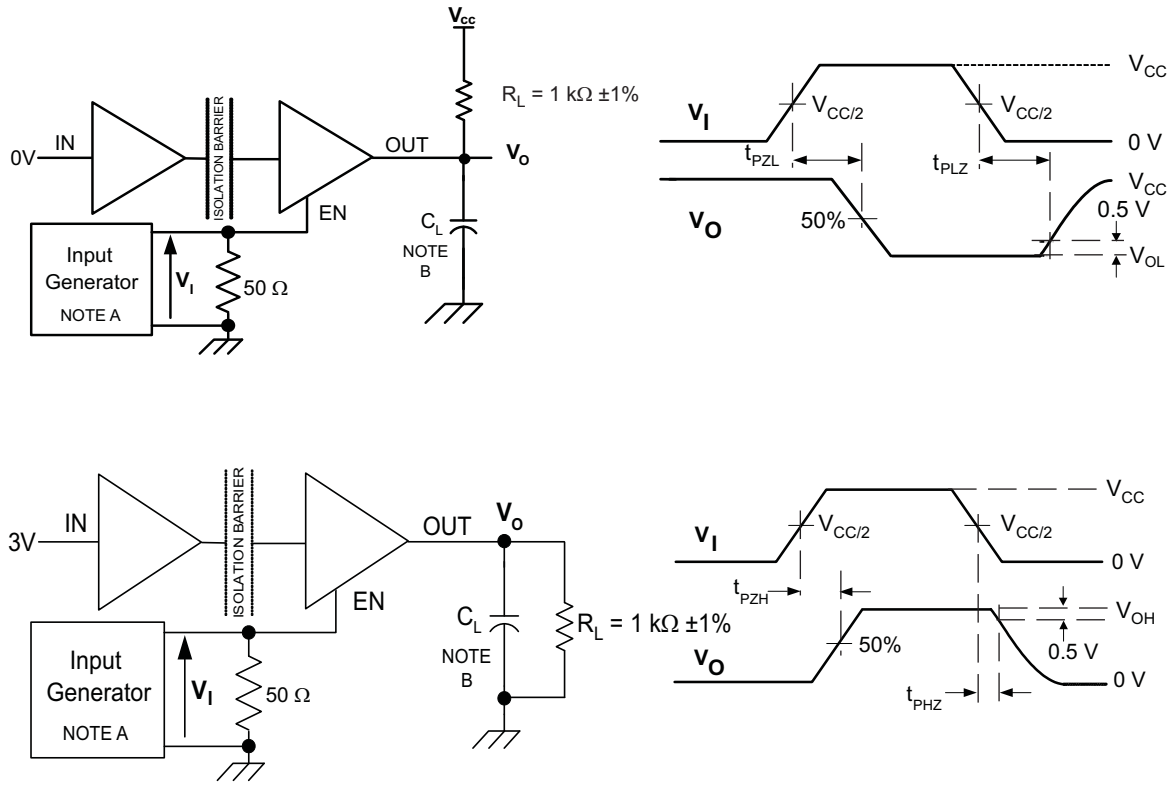
## PARAMETER MEASUREMENT INFORMATION




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms**

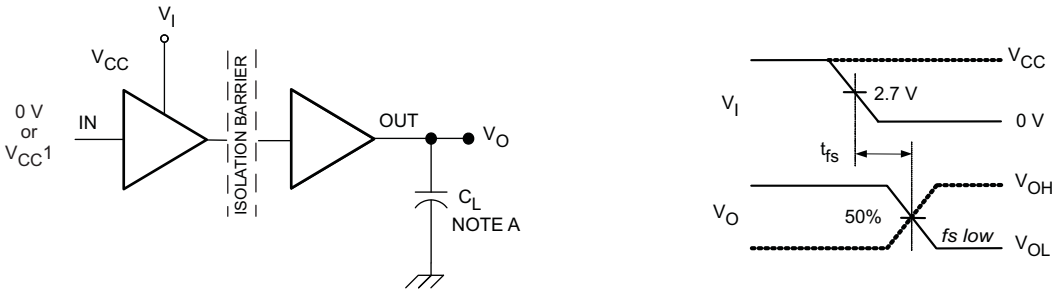



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

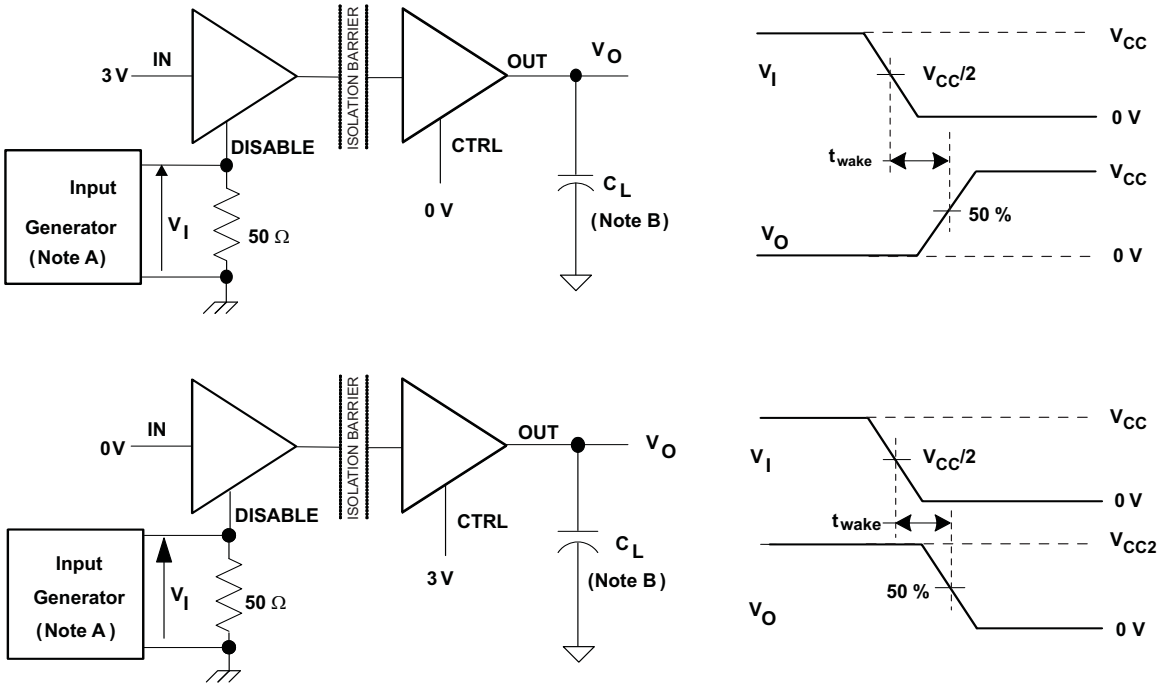
**Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

## PARAMETER MEASUREMENT INFORMATION (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms**



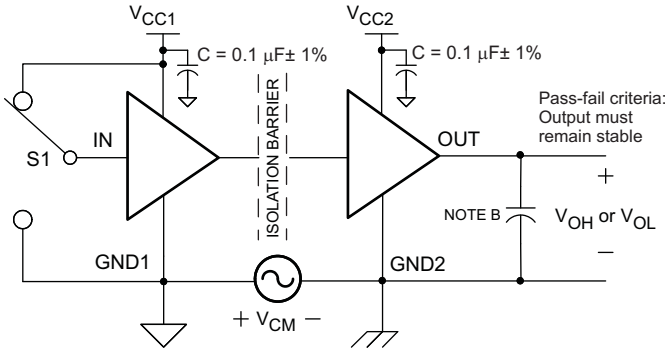

**NOTE: Which ever test yields the longest time is used in this data sheet**

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 4. Wake Time From Input Disable Test Circuit and Voltage Waveforms**

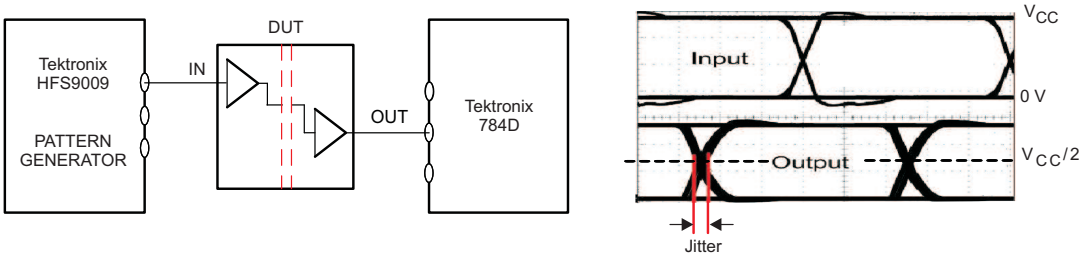
## PARAMETER MEASUREMENT INFORMATION (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

**Figure 5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform**




NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

**Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform**

## DEVICE INFORMATION

### PACKAGE CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (Clearance) | Shortest terminal-to-terminal distance through air | 8.34 | | | mm |
| L(I02) | Minimum external tracking (Creepage) | Shortest terminal-to-terminal distance across the package surface | 8.1 | | | mm |
| CTI | Tracking resistance (comparative tracking index) | DIN IEC 60112/VDE 0303 Part 1 | ≥ 400 | | | V |
| | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| $R_{IO}$ | Isolation resistance | Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device | | >$10^{12}$ | | Ω |
| $C_{IO}$ | Barrier capacitance Input to output | $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |
| $C_I$ | Input capacitance to ground | $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |

### IEC 60664-1 RATINGS TABLE

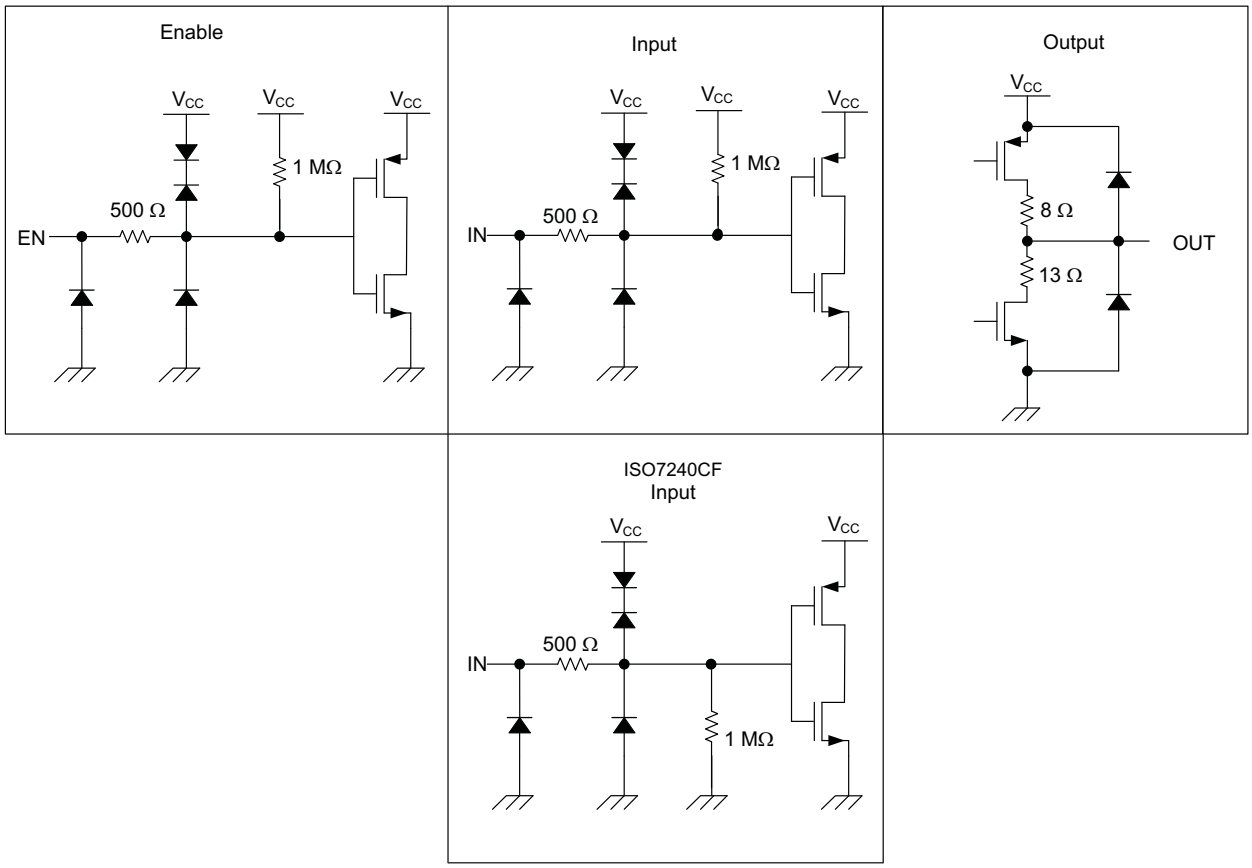
| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|---|---|---|
| Basic isolation group | Material group | II |
| Installation classification | Rated mains voltage ≤150 $V_{RMS}$ | I-IV |
| | Rated mains voltage ≤300 $V_{RMS}$ | I-III |

## REGULATORY INFORMATION

| VDE | CSA | UL |
|---|---|---|
| Certified according to IEC 60747-5-2 | Approved under CSA Component Acceptance Notice 5A | Recognized under 1577 Component Recognition Program |
| Basic Insulation<br>Maximum Transient Overvoltage, 4000 $V_{PK}$<br>Maximum Surge Votlage, 4000 $V_{PK}$<br>Maximum Working Voltage, 560 $V_{PK}$ | Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 395 $V_{RMS}$ maximum working voltage, 4000 $V_{PK}$ maximum isolation rating | Single protection, 2500 $V_{RMS}$ (1) |
| File Number: 40016131 | File Number: 220991 | File Number: E181974 |

(1) Production tested ≥ 3000 $V_{RMS}$ for 1 second in accordance with UL 1577.

## DEVICE I/O SCHEMATICS



## THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-air | Low-K Thermal Resistance(1) | | 168 | | °C/W |
| | | High-K Thermal Resistance | | 96.1 | | |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | | | 61 | | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | | | 48 | | °C/W |
| $P_D$ | Device Power Dissipation | $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, Input a 50% duty cycle square wave | | | 220 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | SOIC-8 | $\theta_{JA} = 212$°C/W, $V_I = 5.5$ V, $T_J = 170$°C, $T_A = 25$°C | | | 156 | mA |
| | | | $\theta_{JA} = 212$°C/W, $V_I = 3.6$ V, $T_J = 170$°C, $T_A = 25$°C | | | 239 | |
| $T_S$ | Maximum case temperature | SOIC-8 | | | | 150 | °C |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

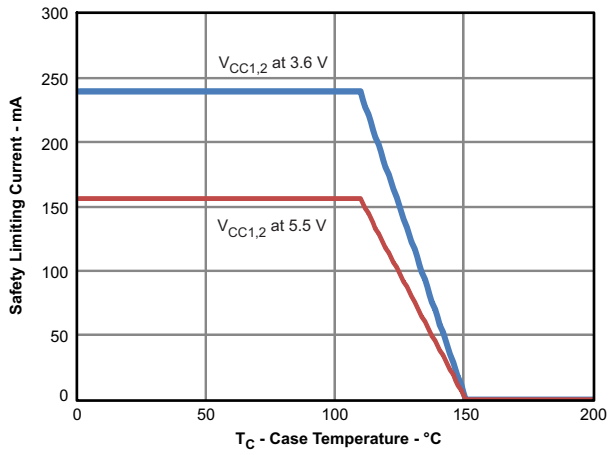



**Figure 7. SOIC-8 $\theta_{JC}$ THERMAL DERATING CURVE per IEC 60747-5-2**

## TYPICAL CHARACTERISTIC CURVES

**ISO7240C/M RMS SUPPLY CURRENT vs SIGNALING RATE**

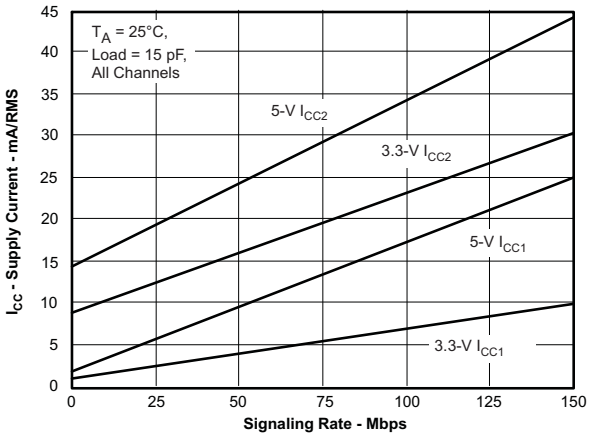



**Figure 8.**

**ISO7241C/M RMS SUPPLY CURRENT vs SIGNALING RATE**

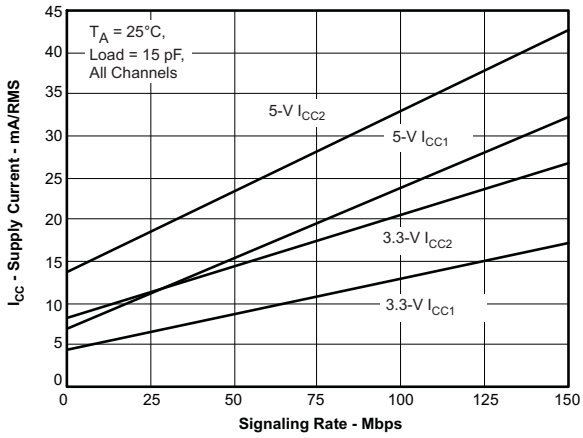



**Figure 9.**

**ISO7242C/M RMS SUPPLY CURRENT vs SIGNALING RATE**

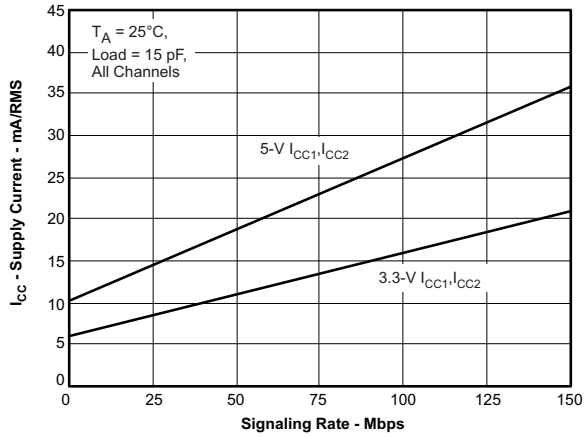



**Figure 10.**

**PROPAGATION DELAY vs FREE-AIR TEMPERATURE**

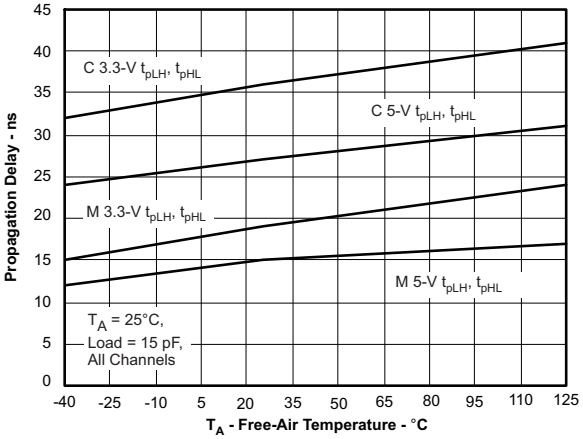



**Figure 11.**

## TYPICAL CHARACTERISTIC CURVES (continued)

**INPUT VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE**

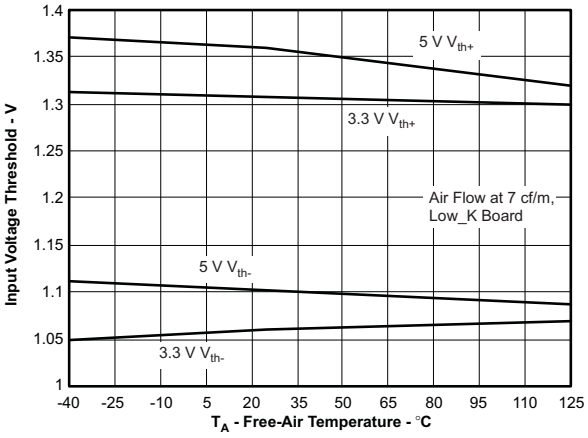



**Figure 12.**

**$V_{CC}$ UNDERVOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE**

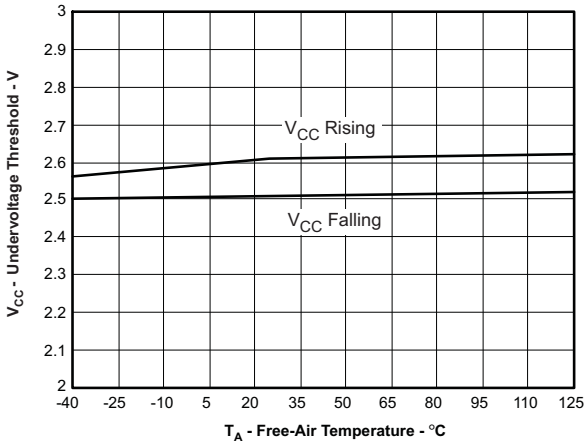



**Figure 13.**

**HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

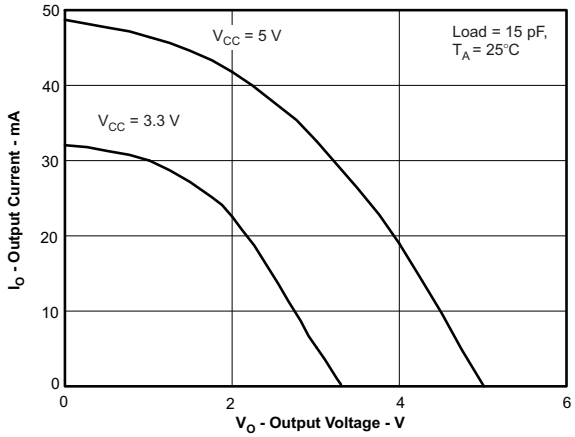



**Figure 14.**

**LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

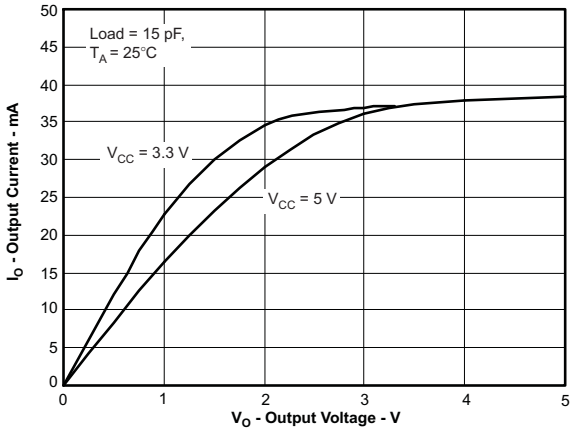



**Figure 15.**

## APPLICATION INFORMATION

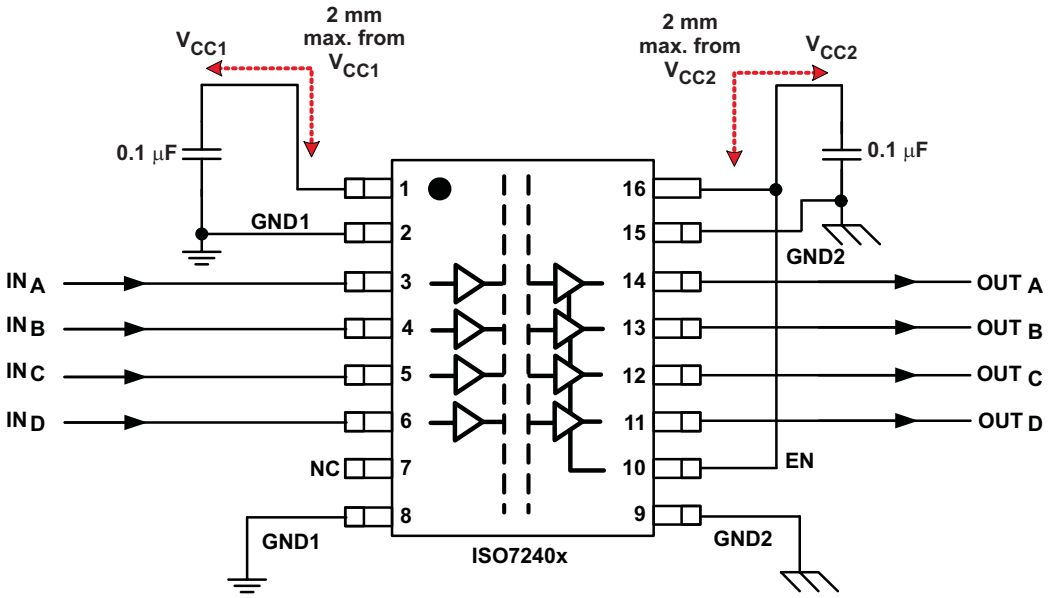



**Figure 16. Typical ISO7240x Application Circuit**

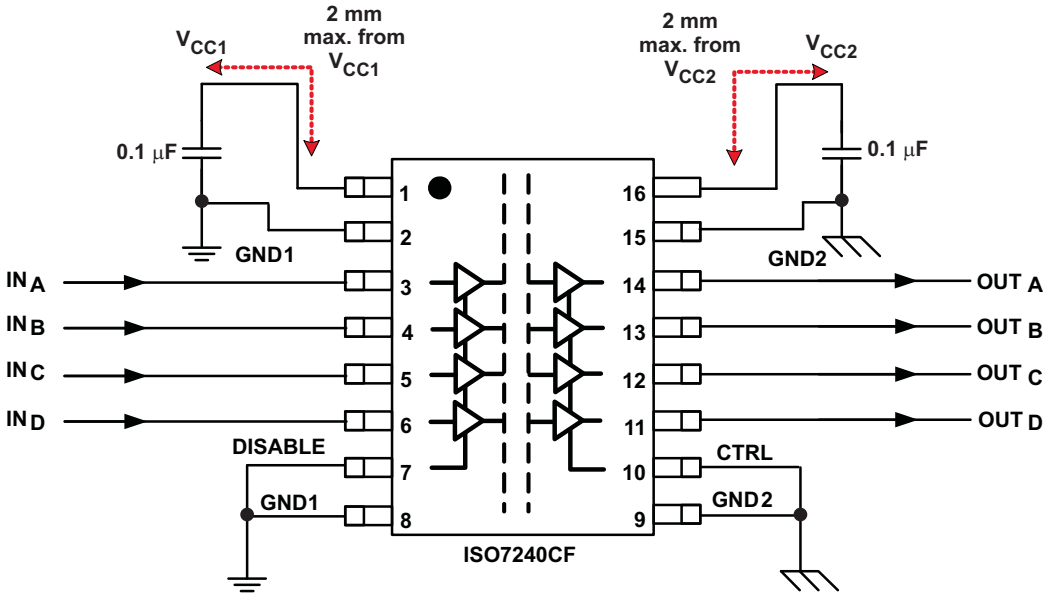



**Figure 17. Typical ISO7240CF Failsafe-Low Application Circuit**

### LIFE EXPECTANCY vs. WORKING VOLTAGE

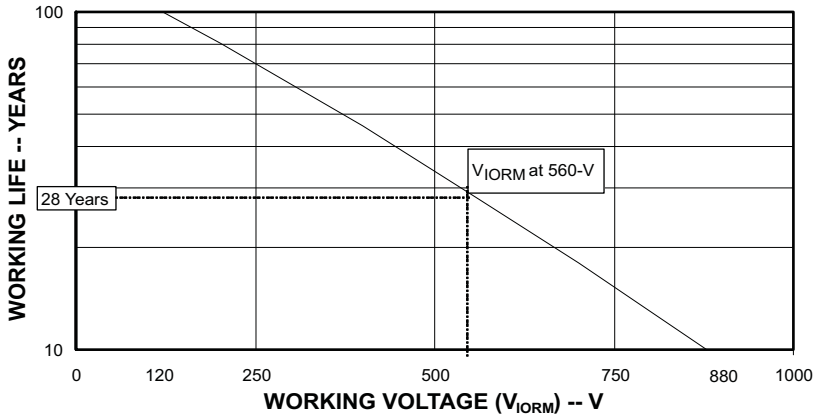



**Figure 18. Time-Dependant Dielectric Breakdown Testing Results**

## REVISION HISTORY

**Changes from Original (September 2007) to Revision A** — **Page**

- Deleted Product Preview note ..... 2
- Changed $V_{CC}$ Supply Voltage in the ROC Table From: 3.6 To: 3.45 ..... 3
- Changed $V_{CC}$ Supply Voltage in the ROC Table From: 3 To: 3.15 ..... 3
- Changed TBDs to actual values. ..... 4
- Changed $C_I$ - typ value From: 1 To: 2 ..... 4
- Changed Propagation delay max From: 22 To: 23 ..... 5
- Changed $C_I$ - typ value From: 1 To: 2 ..... 6
- Changed Propagation delay max From: 46 To: 50 ..... 7
- Changed Propagation delay max From: 28 To: 29 ..... 7
- Changed ISO724xA/C max value From: 2.5 To: 3 ..... 7
- Changed $C_I$ - typ value From: 1 To: 2 ..... 8
- Changed Propagation delay max From: 26 To: 30 ..... 9
- Changed typ value From: 1 To: 2 ..... 10
- Changed Propagation delay max From: 32 To: 34 ..... 11
- Changed ISO724xA/C max value From: 3 To: 3.5 ..... 11
- Changed $C_{IO}$ - typ value From: 1 To: 2 ..... 16
- Changed $C_I$ - typ value From: 1 To: 2 ..... 16
- Changed the REGULATORY INFORMATION Table ..... 17
- Changed Figure 8, Figure 9, and Figure 11. Added Figure 10. ..... 19

**Changes from Revision A (December 2007) to Revision B** — **Page**

- Changed $V_{CC}$ Supply Voltage in the ROC Table From: 3.45 To: 3.6 ..... 3

**Changes from Revision B (August 2008) to Revision C** — **Page**

- Deleted Min = 4.5 V and max = 5.5 V for Supply Voltage of the ROC Table. ..... 3
- Changed $V_{CC}$ Supply Voltage in the ROC Table From: 3.6 To: 5.5 ..... 3

**Changes from Revision C (April 2008) to Revision D** **Page**

- Changed Feature Bullet 4000-$V_{peak}$ Isolation ..... 1
- Added $t_{sk(pp)}$ Part-to-part skew ..... 5
- Added $t_{sk(pp)}$ Part-to-part skew ..... 7
- Added $t_{sk(pp)}$ Part-to-part skew ..... 9
- Added $t_{sk(pp)}$ Part-to-part skew ..... 11
- Changed Typical ISO724x Application Circuit Figure 16 ..... 21

**Changes from Revision D (April 2008) to Revision E** **Page**

- Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V. ..... 3
- Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V ..... 6
- Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V ..... 8
- Added Table Note (1): For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V ..... 10

**Changes from Revision E (May 2008) to Revision F** **Page**

- Changed Title From: QUAD DIGITAL ISOLATORS To: HIGH SPEED QUAD DIGITAL ISOLATORS ..... 1
- Deleted ISO724xA devices. See SLLS905 for the ISO7240A, ISO7241A, and ISO7242A. ..... 1
- Changed Feature Low Jitter Content - From: 1, 25, and 150-Mbps Signaling Rate Options To: 25, and 150-Mbps Signaling Rate Options ..... 1
- Added $t_{sk(pp)}$ footnote. ..... 5
- Added $t_{sk(o)}$ footnote. ..... 5
- Added $t_{sk(pp)}$ footnote. ..... 11
- Added $t_{sk(o)}$ footnote. ..... 11

**Changes from Revision F (May 2008) to Revision G** **Page**

- Changed the PACKAGE CHARACTERISTICS table, line , $L_{(IO1)}$ MIN value from7.7mm to 8.34mm ..... 16

**Changes from Revision G (July 2008) to Revision H** **Page**

- Added Device number ISO7240CF. ..... 1
- Added Features Bullet: Selectable Failsafe Output (ISO7240CF) ..... 1
- Changed description paragraph 4 text. ..... 1
- Added for device number ISO7240CF. ..... 2
- Changed $V_I$ in the Abs Max Table From: Voltage at IN, OUT, EN To: Voltage at IN, OUT, EN, DISABLE, CTRL ..... 3
- Added $t_{wake}$, Wake time from input disable ..... 5
- Added $t_{wake}$, Wake time from input disable ..... 7
- Added $t_{wake}$, Wake time from input disable ..... 9
- Added $t_{wake}$, Wake time from input disable ..... 11

**Changes from Revision H (October 2008) to Revision I** **Page**

- Added information to the Features bullet to include CSA and IEC 60950-1 certification ..... 1

**Changes from Revision I (December 2008) to Revision J** **Page**

- Changed $I_{CC1}$ for Quiescent and 1Mbps From: 10mA To: 11mA ..... 4
- Changed $I_{CC1}$ for Quiescent and 1Mbps From: 10mA To: 11mA ..... 6

**Changes from Revision J (April 2009) to Revision K** **Page**

- Changed the Input circuit in the DEVICE I/O SCHEMATICS illustration ..... 17

**Changes from Revision K (Decemberl 2009) to Revision L** **Page**

- Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table ..... 3
- Added CTI - Tracking resistance (comparative tracking index to the PACKAGE CHARACTERISTICS table ..... 16
- Added the IEC 60664-1 RATINGS TABLE ..... 16

**Changes from Revision L (January 2010) to Revision M** **Page**

- Changed Figure 1, Figure 3, and Figure 4 ..... 14
- Changed the CSA File Number From: 1698195 To: 220991 ..... 17

**Changes from Revision M (January 2011) to Revision N** **Page**

- Changed Feature From: 4000-$V_{peak}$ Isolation, 560-$V_{peak}$ $V_{IORM}$ To: 4000-$V_{peak}$ $V_{IOTM}$, 560-$V_{peak}$ $V_{IORM}$ per IEC 60747-5-2 (VDE 0884, Rev 2) ..... 1
- Changed Feature From: Operates 3.3-V or 5-V Supplies To: Operates With 2.8-V (ISO7241C), 3.3-V or 5-V Supplies ..... 1
- Added device options to $V_{CC}$ in the RECOMMENDED OPERATING CONDITIONS table ..... 3
- Changed Table Note (1) ..... 3
- Changed $I_{CC1}$ and $I_{CC2}$ test conditions in the $V_{CC1}$ and $V_{CC2}$ at 5-V table ..... 4
- Changed Table Note (1) ..... 4
- Changed $I_{CC1}$ and $I_{CC2}$ test conditions in the $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V table ..... 6
- Changed Table Note (1) ..... 6
- Changed $I_{CC1}$ and $I_{CC2}$ test conditions in the $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V table ..... 8
- Changed Table Note (1) ..... 8
- Changed $I_{CC1}$ and $I_{CC2}$ test conditions in the $V_{CC1}$ and $V_{CC2}$ at 3.3 V table ..... 10
- Changed Table Note (1) ..... 10
- Added ELECTRICAL and Switching CHARACTERISTICS tables for$V_{CC1}$ and $V_{CC2}$ at 2.8V (ISO722xC-only) ..... 12
- Changed the CTI MIN value From: ≥175 V To:≥400 V ..... 16
- Changed the REGULATORY INFORMATION Table ..... 17
- Changed Figure 13 From $V_{CC1}$ Failsafe Threshold To: $V_{CC}$ Undervoltage Threshold ..... 19

**Changes from Revision N (January 2012) to Revision O** **Page**

- Added the IEC SAFETY LIMITING VALUES section ..... 18

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7240CDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240C | Samples |
| ISO7240CDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240C | Samples |
| ISO7240CDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240C | Samples |
| ISO7240CDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240C | Samples |
| ISO7240CFDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240CF | Samples |
| ISO7240CFDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240CF | Samples |
| ISO7240CFDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240CF | Samples |
| ISO7240MDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240M | Samples |
| ISO7240MDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240M | Samples |
| ISO7240MDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240M | Samples |
| ISO7240MDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7240M | Samples |
| ISO7241CDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241C | Samples |
| ISO7241CDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241C | Samples |
| ISO7241CDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241C | Samples |
| ISO7241CDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241C | Samples |
| ISO7241MDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241M | Samples |
| ISO7241MDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241M | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7241MDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241M | Samples |
| ISO7241MDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7241M | Samples |
| ISO7242CDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242C | Samples |
| ISO7242CDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242C | Samples |
| ISO7242CDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242C | Samples |
| ISO7242MDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242M | Samples |
| ISO7242MDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242M | Samples |
| ISO7242MDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242M | Samples |
| ISO7242MDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7242M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :**

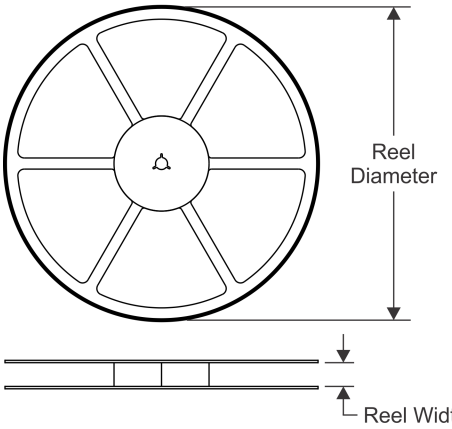
- Automotive: ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1

NOTE: Qualified Version Definitions:

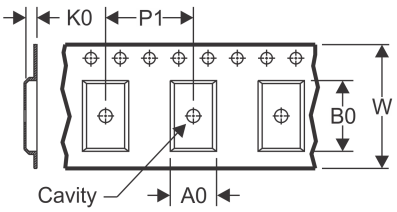
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

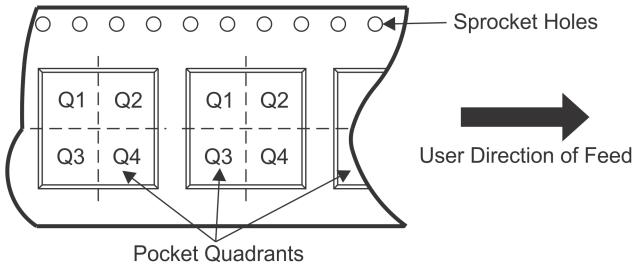



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

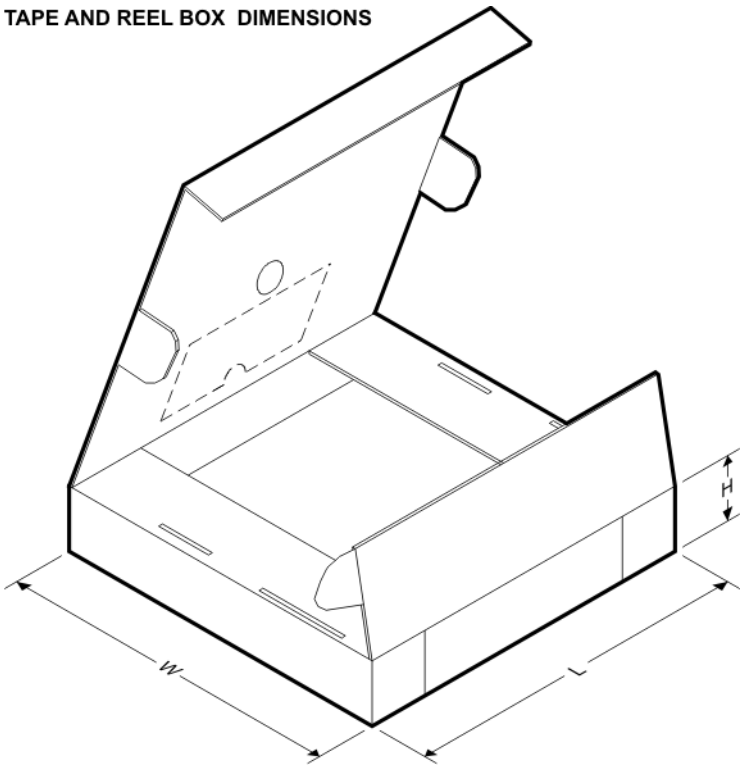
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7240CDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7240CFDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7240MDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7241CDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7241MDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7242CDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7242MDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

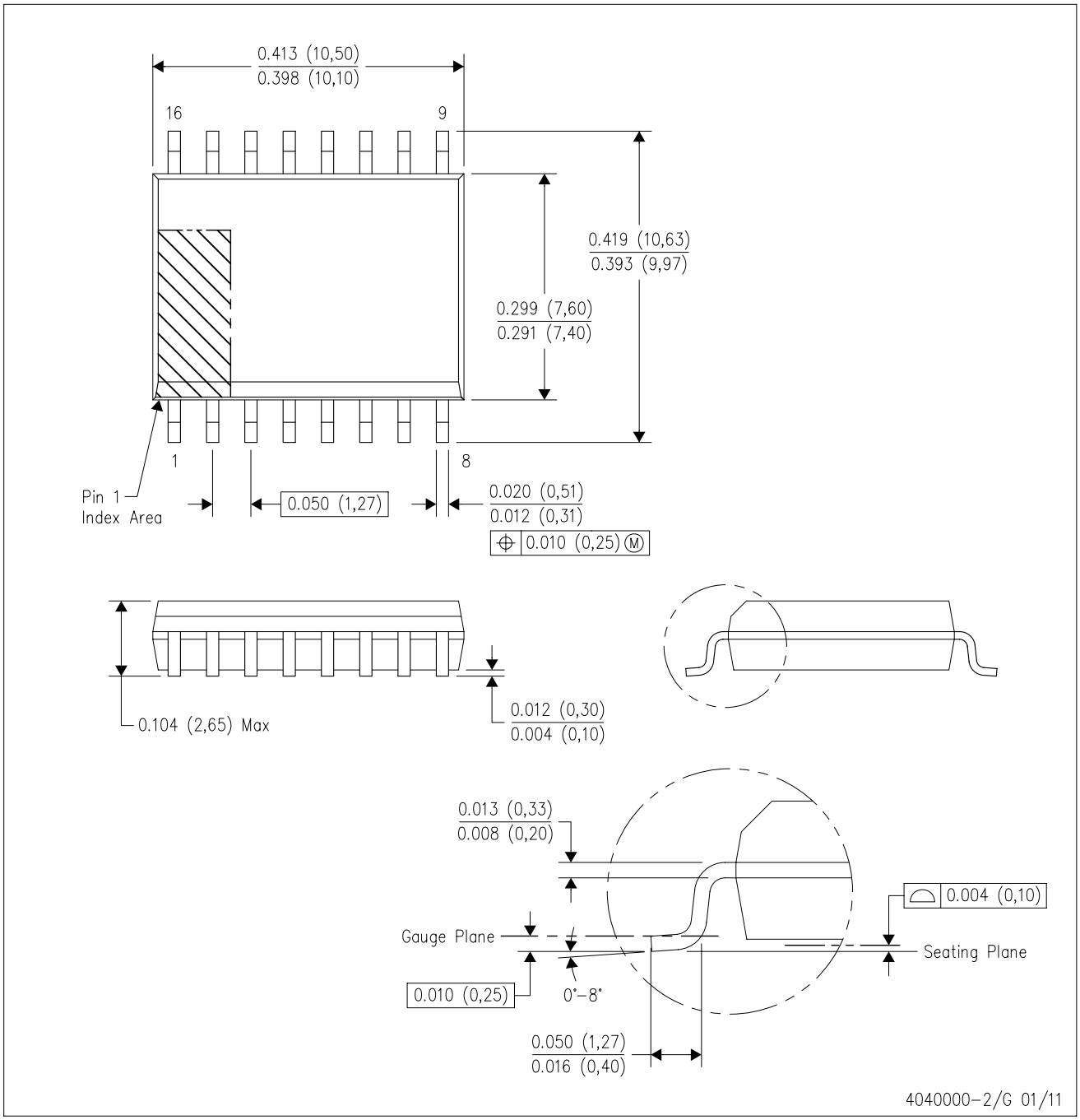
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

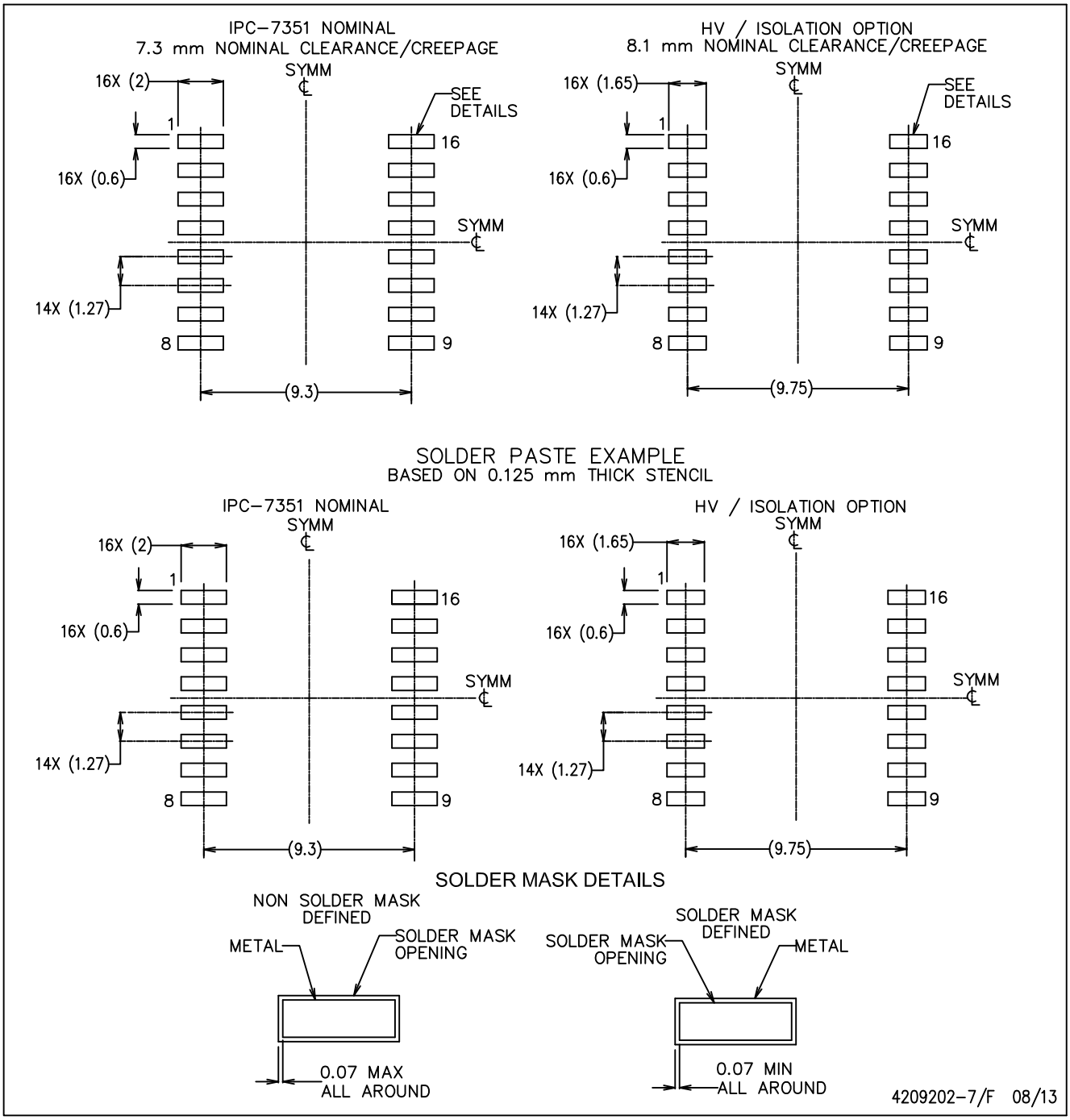
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7240CDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7240CFDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7240MDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7241CDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7241MDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7242CDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7242MDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

# DW (R-PDSO-G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
F. Board assembly site may have different recommendations for stencil design.

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| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
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