XICOR

X5083

CPU Supervisor with 8Kb SPI EEPROM

FEATURES

- **Selectable Timeout Watchdog Timer**
- **Low Vcc Detection and Reset Assertion**
  - **—Five Standard Reset Threshold Voltages**
  - **—Re-program Low Vcc Reset Threshold Voltage using special programming sequence.**
  - **—Reset Signal Valid to Vcc=1V**
- **Long Battery Life With Low Power Consumption**
  - **—<50μA Max Standby Current, Watchdog On**
  - **—<1μA Max Standby Current, Watchdog Off**
  - **—<400μA Max Active Current during Read**
- **1.8V to 3.6V, 2.7V to 5.5V and 4.5V to 5.5V Power Supply Versions**
- **8Kbits of EEPROM—1M Write Cycle Endurance**
- **Save Critical Data With Block Lock™ Memory**
  - **—Block Lock First or Last Page, any 1/4 or Lower 1/2 of E^{2}PROM Array**
- **Built-in Inadvertent Write Protection**
  - **—Write Enable Latch**
  - **—Write Protect Pin**
- **3.3MHz Clock Rate**
- **Minimize Programming Time**
  - **—16 Byte Page Write Mode**
  - **—Self-Timed Write Cycle**
  - **—5ms Write Cycle Time (Typical)**
- **SPI Modes (0,0 & 1,1)**
- **Available Packages**
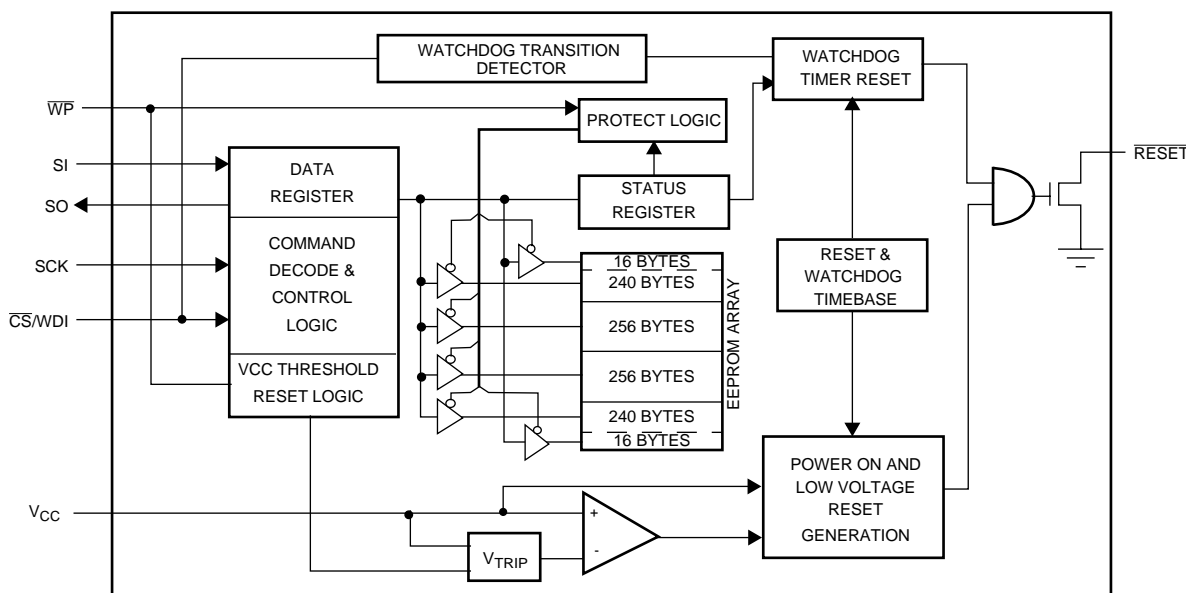 - **—8-Lead TSSOP, 8-Lead SOIC**

DESCRIPTION

This device combines four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power on reset circuit which holds $\overline{RESET}$ active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable timeout interval, the device activates the $\overline{RESET}$ signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low Vcc detection circuitry protects the user's system from low voltage conditions, resetting the system when Vcc falls below the minimum Vcc trip point. $\overline{RESET}$ is asserted until Vcc returns to the proper operating level and stabilizes. Five industry standard V_{TRIP} thresholds are available, however, Xicor's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.
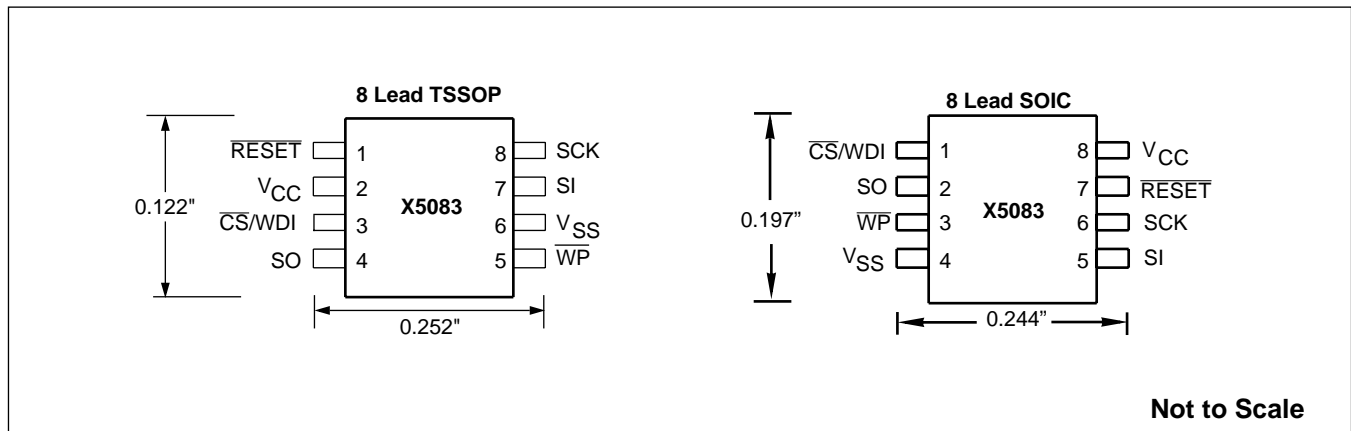
Block Diagram

Characteristics subject to change without notice

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PIN DESCRIPTION

PIN (SOIC/PDIP)	PIN TSSOP	Name	Function
1	1	$\overline{CS}$/WDI	**Chip Select Input.** $\overline{CS}$ HIGH, deselects the device and the SO output pin is at a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power up, a HIGH to LOW transition on $\overline{CS}$ is required. **Watchdog Input.** A HIGH to LOW transition on the WDI pin restarts the Watchdog timer. The absence of a HIGH to LOW transition within the watchdog time-out period results in $\overline{RESET}$ going active.
2	2	SO	**Serial Output.** SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
5	8	SI	**Serial Input.** SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
6	9	SCK	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or data bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
3	6	$\overline{WP}$	**Write Protect.** When $\overline{WP}$ is LOW, nonvolatile write operations to the memory are prohibited. This "Locks" the memory to protect it against inadvertent changes when $\overline{WP}$ is HIGH, the device operates normally.
4	7	V_{SS}	**Ground**
8	14	V_{CC}	**Supply Voltage**
7	13	$\overline{RESET}$	**Reset Output.** $\overline{RESET}$ is an active LOW, open drain output which goes active whenever Vcc falls below the minimum Vcc sense level. It will remain active until Vcc rises above the minimum Vcc sense level for 250ms. $\overline{RESET}$ goes active if the Watchdog Timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the selectable Watchdog time-out period. A falling edge of $\overline{CS}$ will reset the Watchdog Timer. $\overline{RESET}$ goes active on power up at about 1V and remains active for 250ms after the power supply stabilizes.
	3-5,10-12	NC	No internal connections

PIN CONFIGURATION

Not to Scale

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PRINCIPLES OF OPERATION

Power On Reset

Application of power to the X5083 activates a Power On Reset Circuit. This circuit goes LOW at 1V and pulls the $\overline{\text{RESET}}$ pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When Vcc exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{\text{RESET}}$, allowing the processor to begin executing code.

Low voltage monitoring

During operation, the X5083 monitors the V_{CC} level and asserts $\overline{\text{RESET}}$ if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{\text{RESET}}$ signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{\text{RESET}}$ signal remains active until the voltage drops below 1V. It also remains active until Vcc returns and exceeds V_{TRIP} for 200ms.

Watchdog timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the WDI input. The micorprocessor must toggle the $\overline{\text{CS}}$/WDI pin periodically to prevent a $\overline{\text{RESET}}$ signal. The $\overline{\text{CS}}$/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time-out period. The state of two nonvolatile control bits in the Status Register determine the watchdog timer period. The microprocessor can change

these watchdog bits with no action taken by the microprocessor these bits remain unchanged, even after total power failure.

Vcc Threshold Reset Procedure

The X5083 is shipped with a standard Vcc threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X5083 threshold may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.
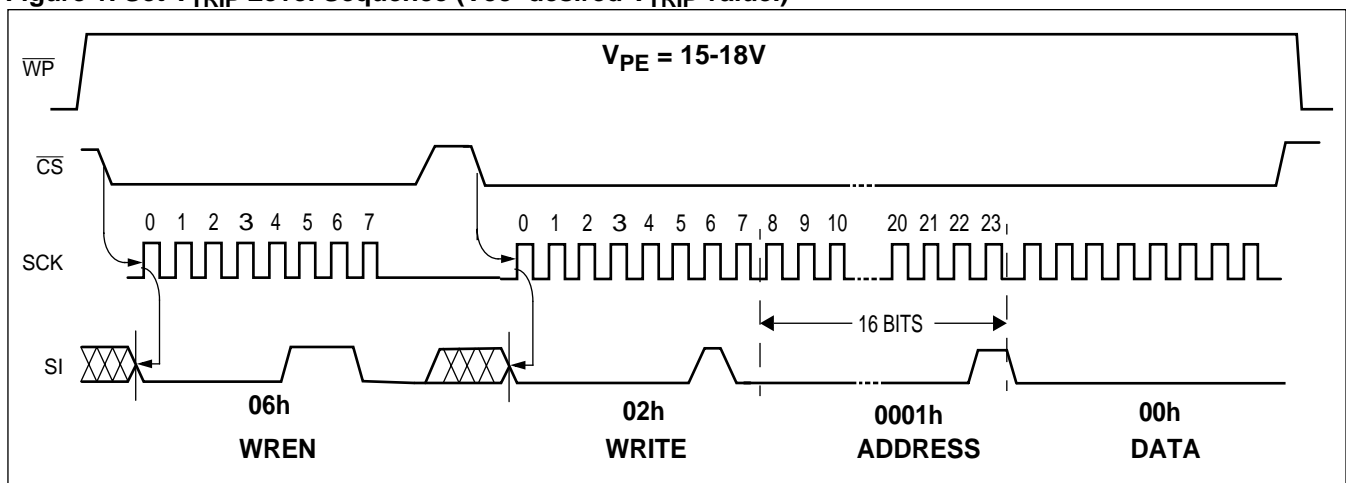
Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the Vcc pin and tie the $\overline{\text{WP}}$ pin to the programming voltage V_P. Then send a WREN command, followed by a write of Data 00h to address 01h. $\overline{\text{CS}}$ going HIGH on the write operation initiates the V_{TRIP} programming sequence. Bring $\overline{\text{WP}}$ LOW to complete the operation.

Note: This operation also writes 00h to array address 01h.

Figure 1. Set V_{TRIP} Level Sequence (Vcc=desired V_{TRIP} value.)

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Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the Vcc pin and tie the $\overline{WP}$ pin to the programming voltage V_P. Then send a WREN command, followed by a write of data 00h to address 03h. $\overline{CS}$ going HIGH on the write operation initiates the V_{TRIP} programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

Note: This operation also writes 00h to array address 03h.

Figure 2. Reset V_{TRIP} Level Sequence (Vcc > 3V. $\overline{WP}$ = 15-18V)
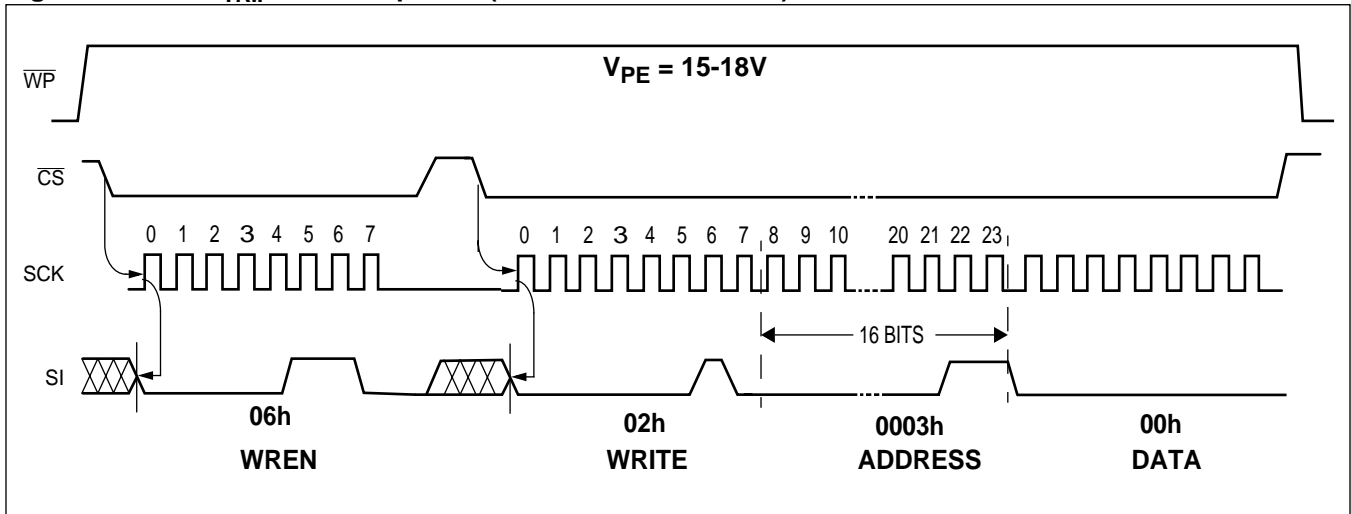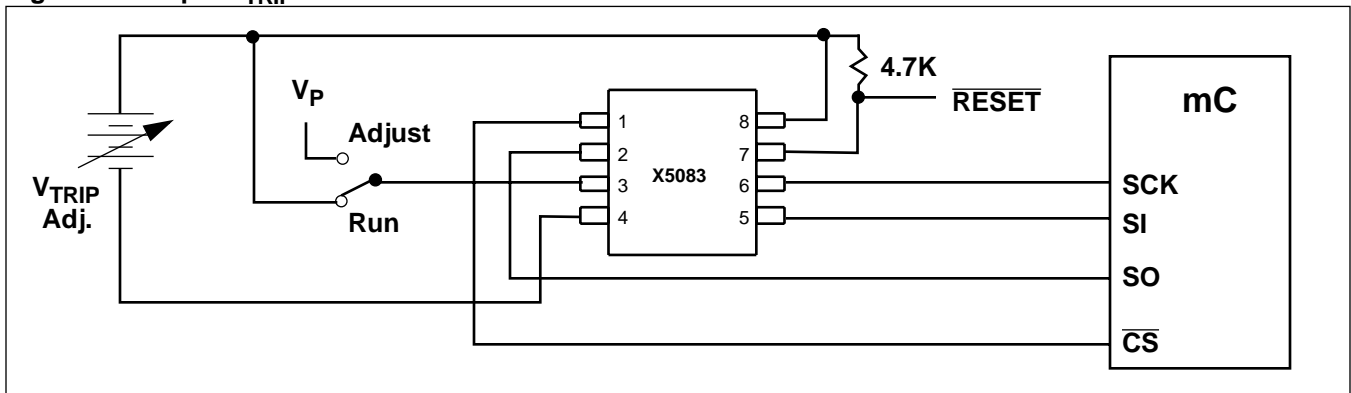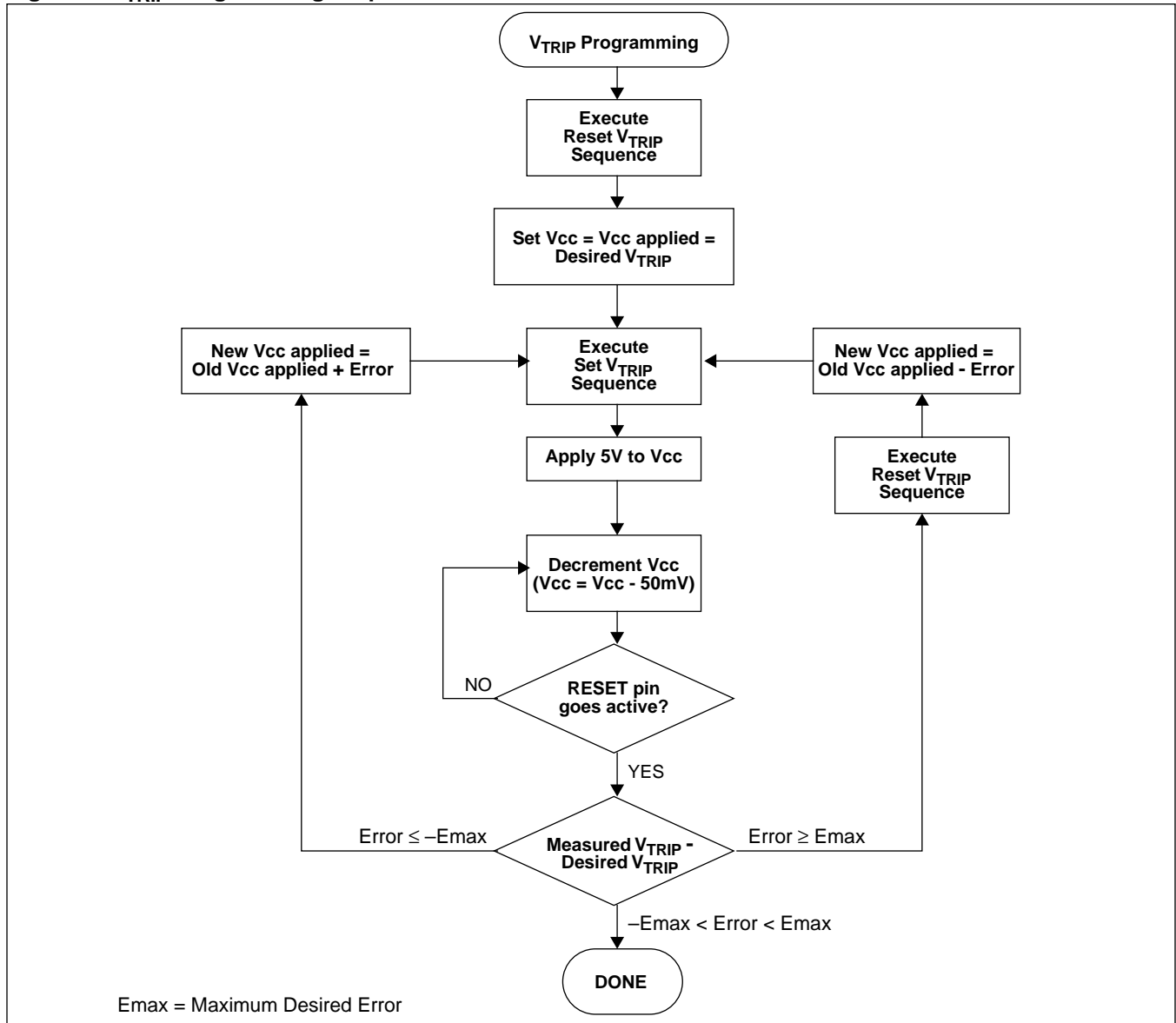

Figure 3. Sample V_{TRIP} Reset Circuit

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Figure 4. V_{TRIP} Programming Sequence

Figure 4. V_{TRIP} Programming Sequence

```
                         ┌─────────────────────┐
                         │  V_TRIP Programming │
                         └─────────────────────┘
                                   │
                         ┌─────────────────────┐
                         │      Execute         │
                         │   Reset V_TRIP       │
                         │    Sequence          │
                         └─────────────────────┘
                                   │
                         ┌─────────────────────┐
                         │ Set Vcc = Vcc applied│
                         │  = Desired V_TRIP    │
                         └─────────────────────┘
                                   │
  ┌──────────────────┐   ┌─────────────────────┐   ┌──────────────────┐
  │ New Vcc applied = │──▶│      Execute        │◀──│ New Vcc applied = │
  │ Old Vcc applied   │   │    Set V_TRIP       │   │ Old Vcc applied   │
  │    + Error        │   │    Sequence         │   │    - Error        │
  └──────────────────┘   └─────────────────────┘   └──────────────────┘
          ▲                        │                         ▲
          │              ┌─────────────────────┐   ┌──────────────────┐
          │              │   Apply 5V to Vcc    │   │     Execute       │
          │              └─────────────────────┘   │   Reset V_TRIP    │
          │                        │                │    Sequence       │
          │              ┌─────────────────────┐   └──────────────────┘
          │         ┌───▶│   Decrement Vcc      │             ▲
          │         │    │ (Vcc = Vcc - 50mV)   │             │
          │         │    └─────────────────────┘             │
          │         │              │                         │
          │         │          ◇───────◇                     │
          │      NO │         ╱ RESET pin ╲                  │
          │         └────────│ goes active? │                │
          │                   ╲            ╱                  │
          │                    ◇─────────◇                   │
          │                        │ YES                     │
          │                    ◇───────◇                     │
  Error ≤ -Emax              ╱ Measured   ╲   Error ≥ Emax    │
          └─────────────────│ V_TRIP -     │─────────────────┘
                             ╲ Desired     ╱
                              ╲ V_TRIP    ╱
                               ◇────────◇
                                   │
                          -Emax < Error < Emax
                                   │
                             ┌──────────┐
                             │   DONE   │
                             └──────────┘

   Emax = Maximum Desired Error
```

SPI Serial Memory

The memory portion of the device is a CMOS Serial EEPROM array with Xicor's Block Lock™ Protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device monitors the bus and asserts $\overline{RESET}$ output if there is no bus activity within user selctable time-out period or the supply voltage falls below a preset minimum V_{TRIP}. The device contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire operation.

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All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

Status Register/Block Lock/WDT Byte

7	6	5	4	3	2	1	0
0	0	0	WD1	WD0	BL2	BL1	BL0

Block Lock Memory

Xicor's Block Lock Memory provides a flexible mechanism to store and lock system ID and parametric information. There are seven distinct Block Lock Memory areas within the array which vary in size from one page to as much as half of the entire array. These areas and associated address ranges are Block Locked by writing the appropriate two byte Block Lock instruction to the device as described in Table 1 and Figure 7. Once a Block Lock instruction has been completed, that Block Lock setup is held in the nonvolatile Status Register until the next Block Lock instruction is issued. The sections of the memory array that are Block Locked can be read but not written until Block Lock is removed or changed.

Table 1. Instruction Set and Block Lock Protection Byte Definition

Instruction Format	Instruction Name and Operation
0000 0110	WREN: Set the Write Enable Latch (Write Enable Operation)
0000 0100	WRDI: Reset the Write Enable Latch (Write Disable Operation)
0000 0001	**Write Status Instruction—followed by:** **Block Lock/WDT Byte: (See Figure 1)** $000 WD_1 WD_2 000$ --->NO Block Lock: 00h-00h- - - >None of the Array $000 WD_1 WD_2 001$ --->Block Lock Q1: 0000h-00FFh>Lower Quadrant (Q1) $000 WD_1 WD_2 010$ --->Block Lock Q2: 0100h-01FFh>Q2 $000 WD_1 WD_2 011$ --->Block Lock Q3: 0200h-02FFh>Q3 $000 WD_1 WD_2 100$ --->Block Lock Q4: 0300h-03FFh>Upper Quadrant (Q4) $000 WD_1 WD_2 101$ --->Block Lock H1: 0000h-01FFh>Lower Half of the Array (H1) $000 WD_1 WD_2 110$ --->Block Lock P0: 0000h-000Fh>Lower Page (P0) $000 WD_1 WD_2 111$ --->Block Lock Pn: 03F0h-03FFh>Upper Page (Pn)
0000 0101	READ STATUS: Reads Status Register & provides write in progress status on SO Pin
0000 0010	WRITE: Write operation followed by address and data
0000 0011	READ: Read operation followed by address

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Watchdog Timer

The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time-out Period. These nonvolatile bits are programmed with the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

Read Sequence

When reading from the E2PROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the Read E2PROM Array Sequence (Figure 1).

To read the Status Register, the $\overline{CS}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the "Write Enable" Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the Write Operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the EEPROM memory array, the user then issues the WRITE instruction followed by the 16 bit address and then the data to be written. Any unused address bits are specified to be "0's". The WRITE operation minimally takes 32 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the same page and overwrite any data that may have been previously written.

For a Write Operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 5, 6 and 7 must be "0".

Read Status Operation

If there is not a nonvolatile write in progress, the Read Status instruction returns the Block Lock setting from the Status Register which contains the Block Lock bits IDL2-IDL0 (Figure 1). The Block Lock bits define the Block Lock condition (Figure 1/Table1). The other bits are reserved and will return '0' when read. See Figure 3.

If a nonvolatile write is in progress, the Read Status Instruction returns a HIGH on SO. When the nonvolatile write cycle is completed, the status register data is read out.

Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (See Figure 3).

$\overline{RESET}$ Operation

The $\overline{RESET}$ output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point and/or the Watchdog timer has reached its programmable time-out limit.

The $\overline{RESET}$ output is an open drain output and requires a pull up resistor.

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Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The Write Enable Latch is reset.
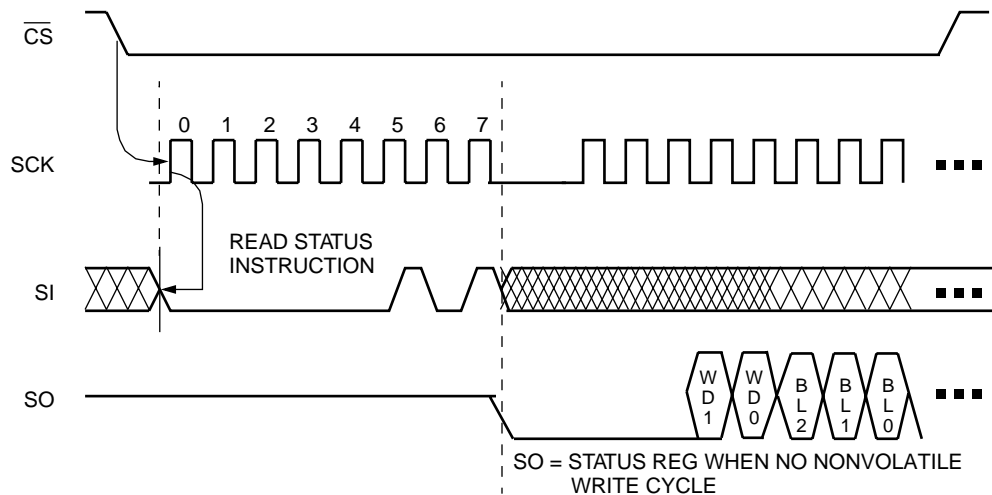- Reset Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

Figure 5. Read Operation Sequence
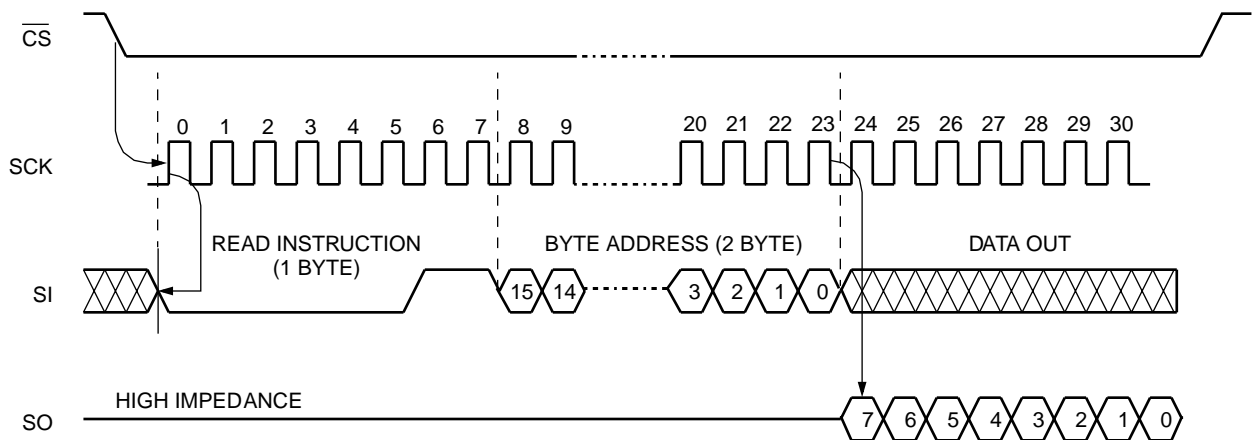
Figure 6. Read Status Operation Sequence

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Figure 7. WREN/WRDI Sequence
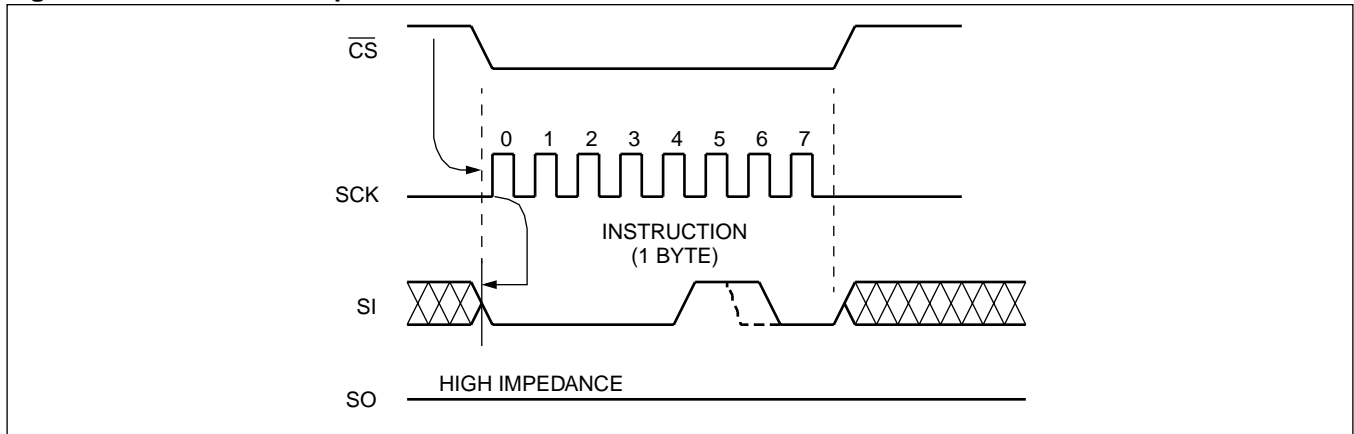
Figure 8. EEPROM Array Write Sequence
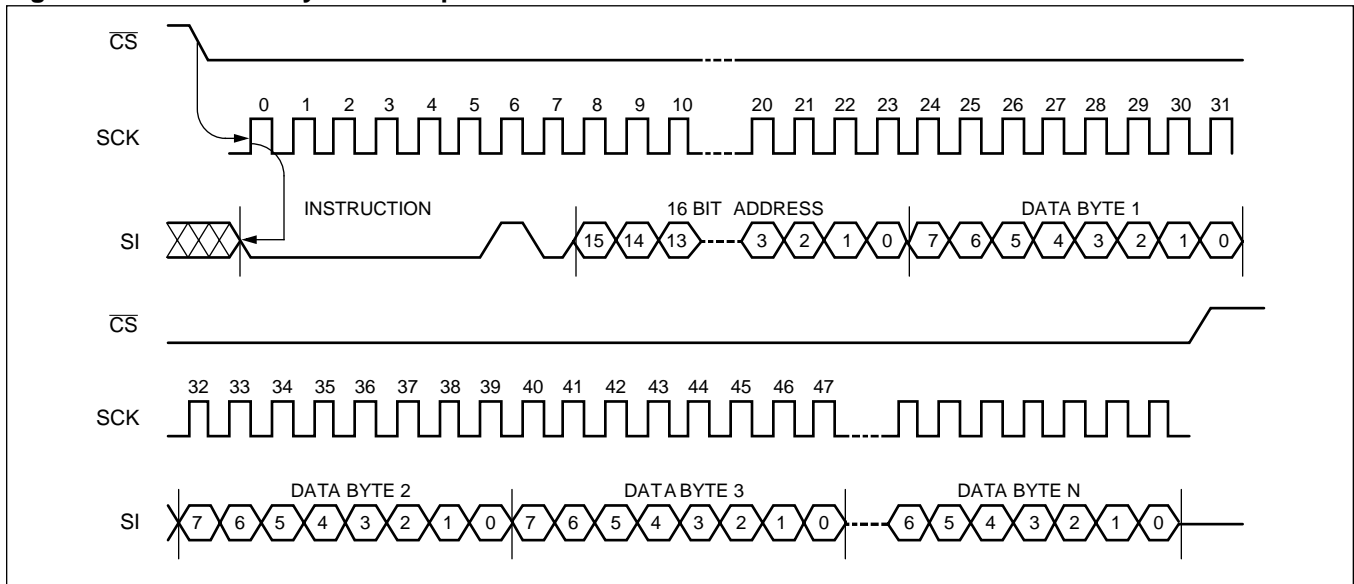
Figure 9. Status Register Write Sequence

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Figure 10. Read Nonvolatile Write Status (Option 1)
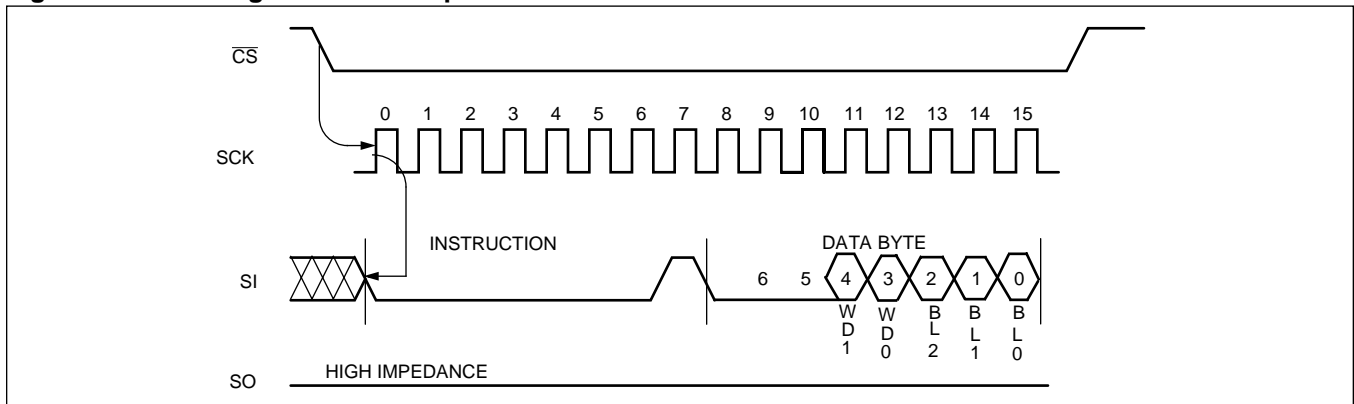
Figure 10. Read Nonvolatile Write Status (Option 1)

Figure 11. Read Nonvolatile Write Status (Option 2)
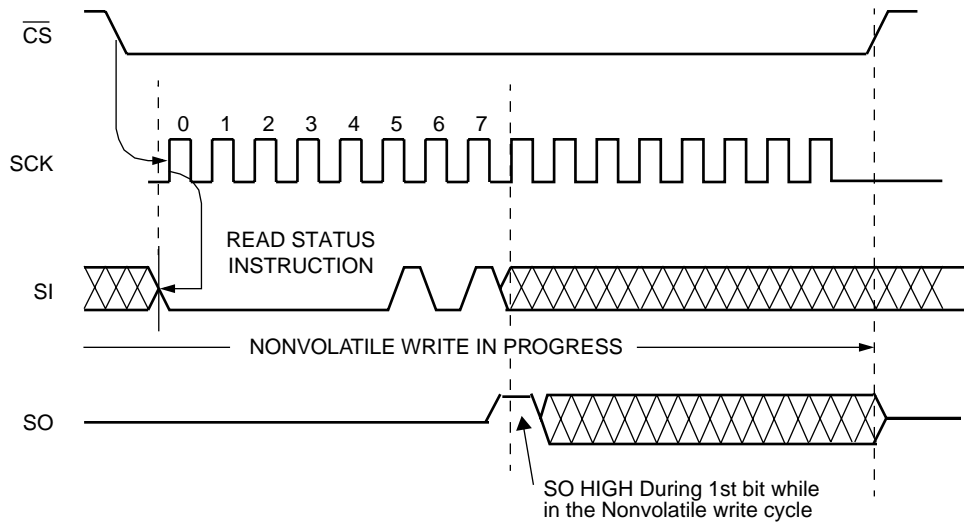
Figure 11. Read Nonvolatile Write Status (Option 2)
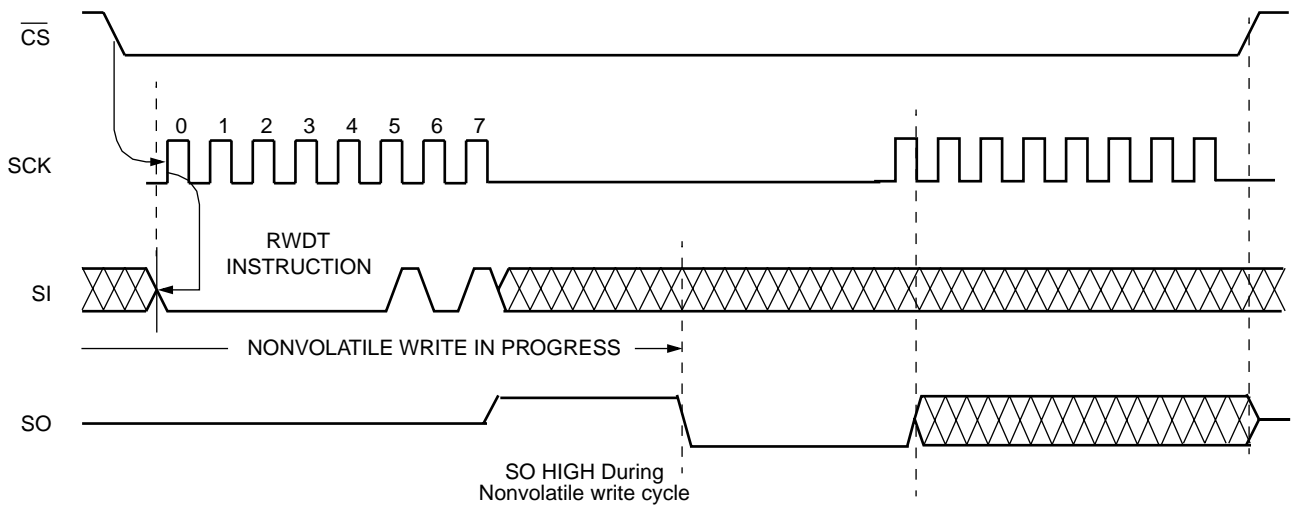
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with Respect to V$_{SS}$ ..−1.0V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 seconds) .... 300°C

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C

7036 FRM T07

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Voltage Option	Limits
−1.8	1.8V-3.6V
−2.7	2.7V to 5.5V
Blank	4.5V-5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I$_{CC1}$	V$_{CC}$ Write Current (Active)			5	mA	SCK = V$_{CC}$ x 0.1/V$_{CC}$ x 0.9 @ 5MHz, SO = Open
I$_{CC2}$	V$_{CC}$ Read Current (Active)			0.4	mA	SCK = V$_{CC}$ x 0.1/V$_{CC}$ x 0.9 @ 5MHz, SO = Open
I$_{SB1}$	V$_{CC}$ Standby Current WDT=OFF			1	μA	$\overline{CS}$ = V$_{CC}$, V$_{IN}$ = V$_{SS}$ or V$_{CC}$, V$_{CC}$ = 5.5V
I$_{SB2}$	V$_{CC}$ Standby Current WDT=ON			50	μA	$\overline{CS}$ = V$_{CC}$, V$_{IN}$ = V$_{SS}$ or V$_{CC}$, V$_{CC}$ = 5.5V
I$_{SB3}$	V$_{CC}$ Standby Current WDT=ON			20	μA	$\overline{CS}$ = V$_{CC}$, V$_{IN}$ = V$_{SS}$ or V$_{CC}$, V$_{CC}$ =3.6V
I$_{LI}$	Input Leakage Current		0.1	10	μA	V$_{IN}$ = V$_{SS}$ to V$_{CC}$
I$_{LO}$	Output Leakage Current		0.1	10	μA	V$_{OUT}$ = V$_{SS}$ to V$_{CC}$
V$_{IL}$[1]	Input LOW Voltage	−0.5		V$_{CC}$x0.3	V	
V$_{IH}$[1]	Input HIGH Voltage	V$_{CC}$x0.7		V$_{CC}$+0.5	V	
V$_{OL1}$	Output LOW Voltage			0.4	V	V$_{CC}$ > 3.3V, I$_{OL}$ = 2.1mA
V$_{OL2}$	Output LOW Voltage			0.4	V	2V < V$_{CC}$ ≤ 3.3V, I$_{OL}$ = 1mA
V$_{OL3}$	Output LOW Voltage			0.4	V	V$_{CC}$ ≤ 2V, I$_{OL}$ = 0.5mA
V$_{OH1}$	Output HIGH Voltage	V$_{CC}$−0.8			V	V$_{CC}$ > 3.3V, I$_{OH}$ = −1.0mA
V$_{OH2}$	Output HIGH Voltage	V$_{CC}$−0.4			V	2V < V$_{CC}$ ≤ 3.3V, I$_{OH}$ = −0.4mA
V$_{OH3}$	Output HIGH Voltage	V$_{CC}$−0.2			V	V$_{CC}$ ≤ 2V, I$_{OH}$ = −0.25mA
V$_{OLRS}$	Reset Output LOW Voltage			0.4	V	I$_{OL}$ = 1mA

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t$_{PUR}$[2]	Power-up to Read Operation		1	ms
t$_{PUW}$[2]	Power-up to Write Operation		5	ms

CAPACITANCE   T$_A$ = +25°C, f = 1MHz, V$_{CC}$ = 5V.

Symbol	Test	Max.	Units	Conditions
C$_{OUT}$[2]	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	V$_{OUT}$ = 0V
C$_{IN}$[2]	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V$_{IN}$ = 0V

Notes: (1) V$_{IL}$ min. and V$_{IH}$ max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

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EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}
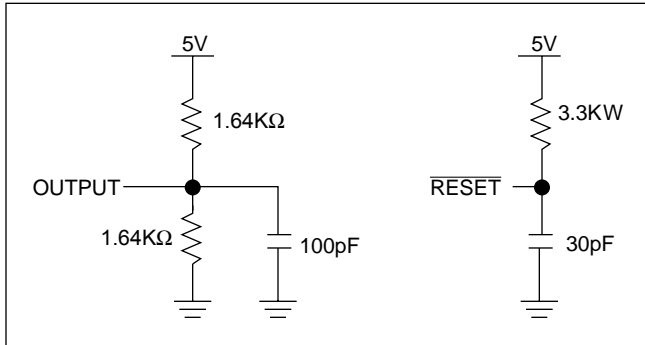
A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	1.8-3.6V		2.7V–5.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock Frequency	0	2	0	3.3	MHz
t_{CYC}	Cycle Time	500		300		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		150		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		150		ns
t_{WH}	Clock HIGH Time	200		130		ns
t_{WL}	Clock LOW Time	200		130		ns
t_{SU}	Data Setup Time	50		20		ns
t_{H}	Data Hold Time	50		20		ns
t_{RI}[3]	Input Rise Time		2		2	µs
t_{FI}[3]	Input Fall Time		2		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	250		100		ns
t_{WC}[4]	Write Cycle Time		10		10	ms

Data Output Timing

Symbol	Parameter	1.8-3.6V		2.7V–5.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock Frequency	0	2	0	3.3	MHz
t_{DIS}	Output Disable Time		250		150	ns
t_{V}	Output Valid from Clock Low		200		130	ns
t_{HO}	Output Hold Time	0		0		ns
t_{RO}[3]	Output Rise Time		100		50	ns
t_{FO}[3]	Output Fall Time		100		50	ns

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing
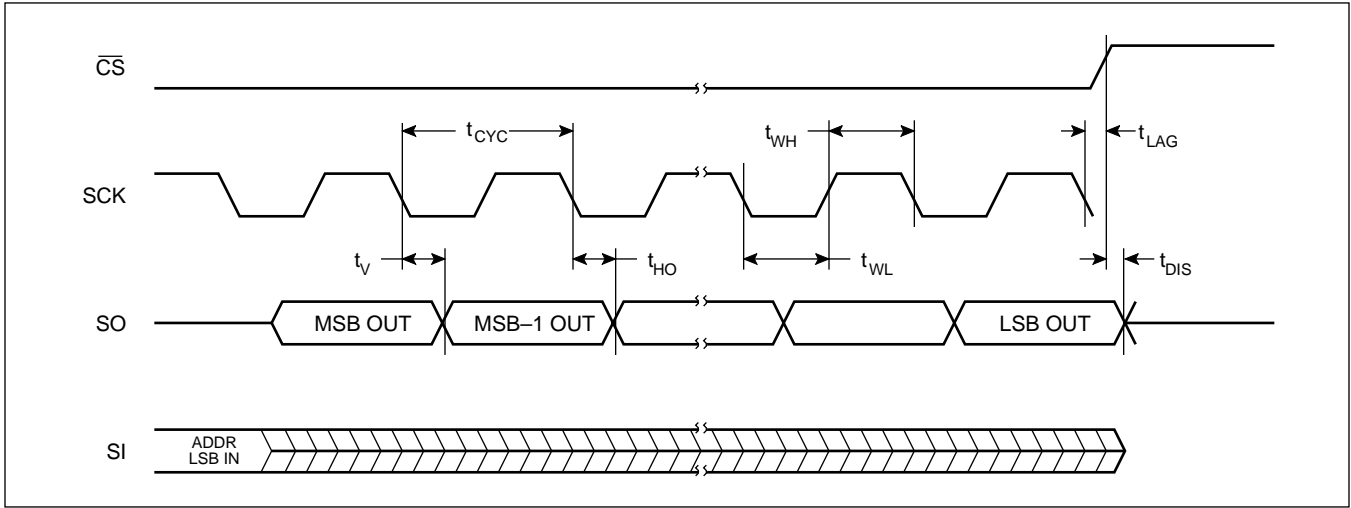
Serial Input Timing
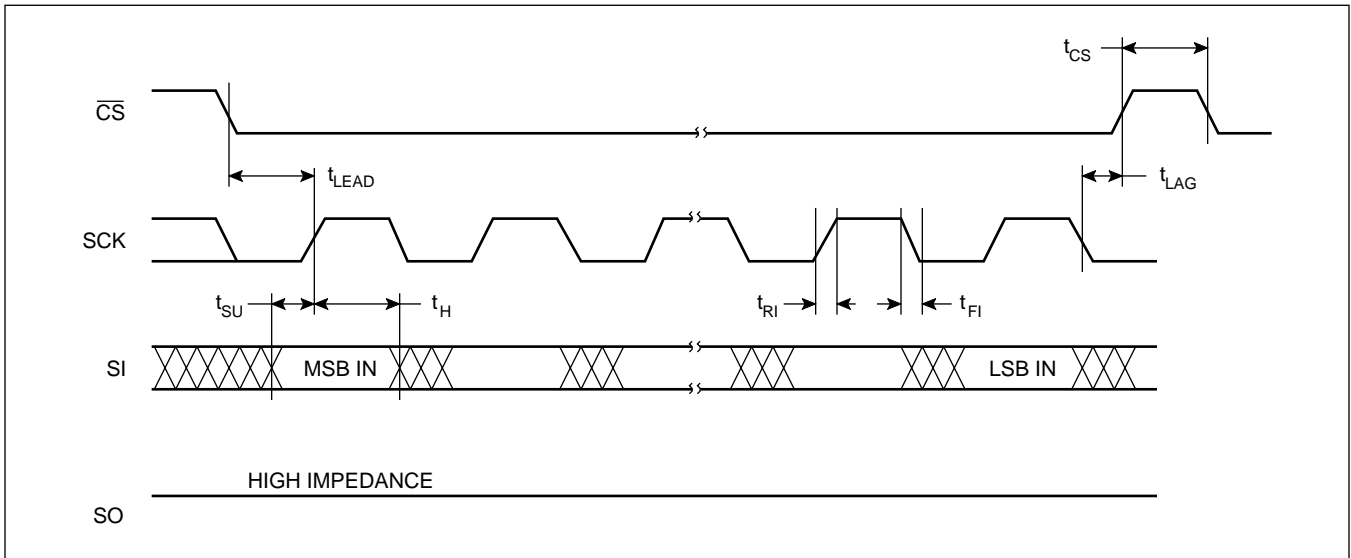
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Power-Up and Power-Down Timing
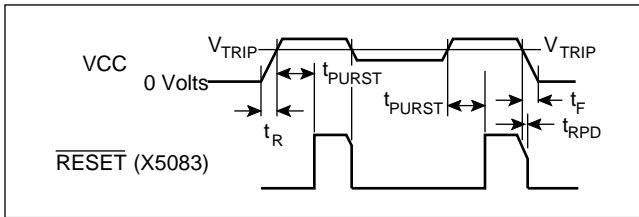
RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	Reset Trip Point Voltage, X5083PT-4.5A Reset Trip Point Voltage, X5083PT Reset Trip Point Voltage, X5083PT-2.7A Reset Trip Point Voltage, X5083PT-2.7 Reset Trip Point Voltage, X5083PT-1.8	4.5 4.25 2.85 2.55 1.7	4.63 4.38 2.93 2.63 1.75	4.75 4.5 3.00 2.7 1.8	V
t_{PURST}	Power-up Reset Timeout	100	200	280	ms
t_{RPD}[5]	V_{CC} Detect to Reset/Output			500	ns
t_F[5]	V_{CC} Fall Time	0.1			ns
t_R[5]	V_{CC} Rise Time	0.1			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

Notes: (5) This parameter is periodically sampled and not 100% tested.
PT= Package/Temperature

CS vs. RESET Timing
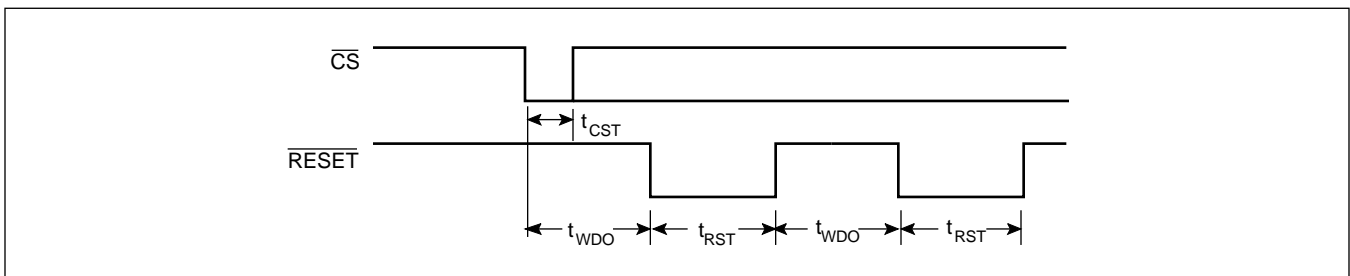
RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period, WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	$\overline{CS}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Timeout	100	200	300	ms

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V_{TRIP} Programming Timing Diagram
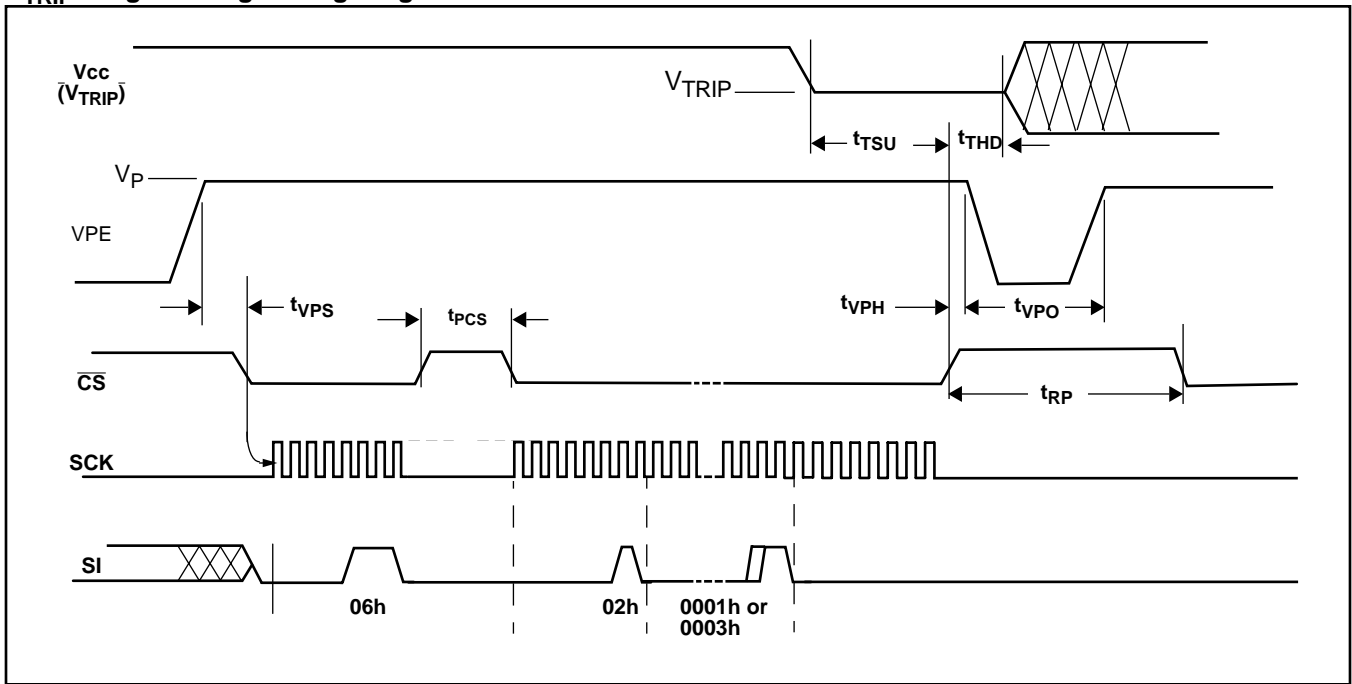
X5083

V_{TRIP} Programming Parameters

Parameter	Description	Min	Max	Units
t_{VPS}	V_{TRIP} Program Enable Voltage Setup time	1		µs
t_{VPH}	V_{TRIP} Program Enable Voltage Hold time	1		µs
t_{PCS}	V_{TRIP} Programming $\overline{CS}$ inactive time	1		µs
t_{TSU}	V_{TRIP} Setup time	1		µs
t_{THD}	V_{TRIP} Hold (stable) time	10		ms
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{VPO}	V_{TRIP} Program Enable Voltage Off time (Between successive adjustments)	0		us
t_{RP}	V_{TRIP} Program Recovery Period (Between successive adjustments)	10		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Programmed Voltage Range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} Program Voltage accuracy (Vcc applied - V_{TRIP}) (Programmed at 25ºC.)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} Program Voltage accuracy [(Vcc applied - V_{ta1}) - V_{TRIP}. Programmed at 25ºC.)	-25	+25	mV
V_{tr}	V_{TRIP} Program Voltage repeatability (Successive program operations. Programmed at 25ºC.)	-25	+25	mV
V_{tv}	V_{TRIP} Program variation after programming (0-75ºC). (Programmed at 25ºC.)	-25	+25	mV

V_{TRIP} Programming parameters are periodically sampled and are not 100% Tested.

X5083

Vcc Supply Current vs. Temperature (I$_{SB}$)
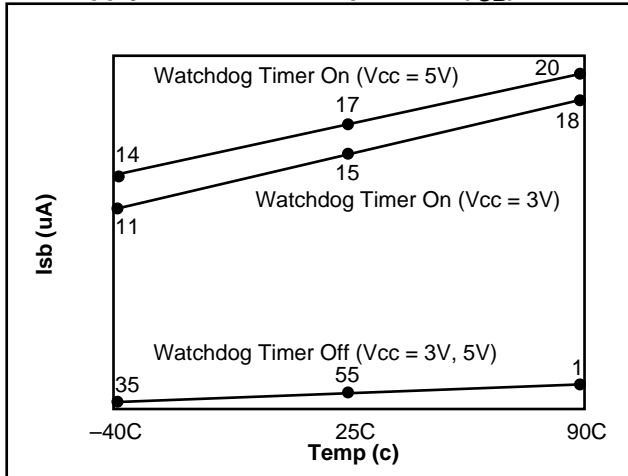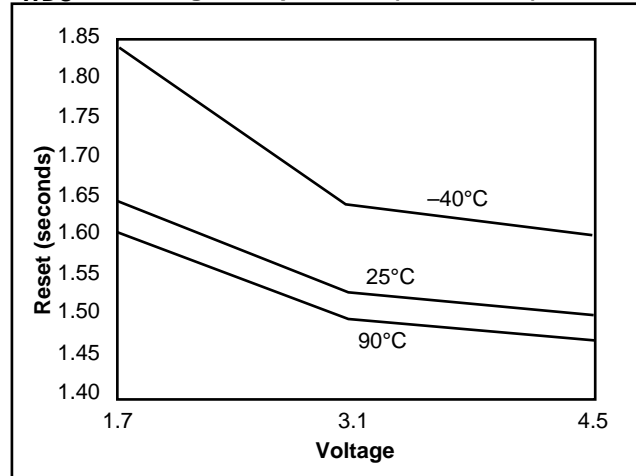
V$_{TRIP}$ vs. Temperature (programmed at 25°C)

t$_{PURST}$ vs. Temperature
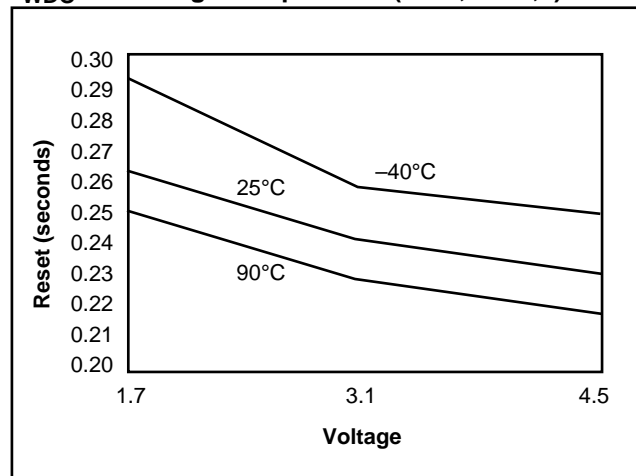

t$_{WDO}$ vs. Voltage/Temperature (WD1,0=1,1)

t$_{WDO}$ vs. Voltage/Temperature (WD1,0=1,0)
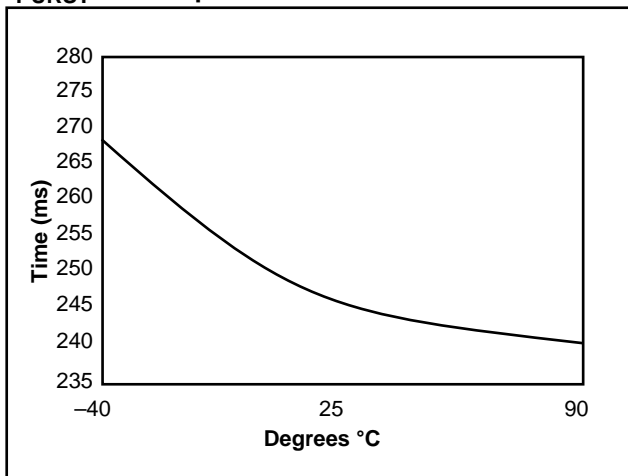
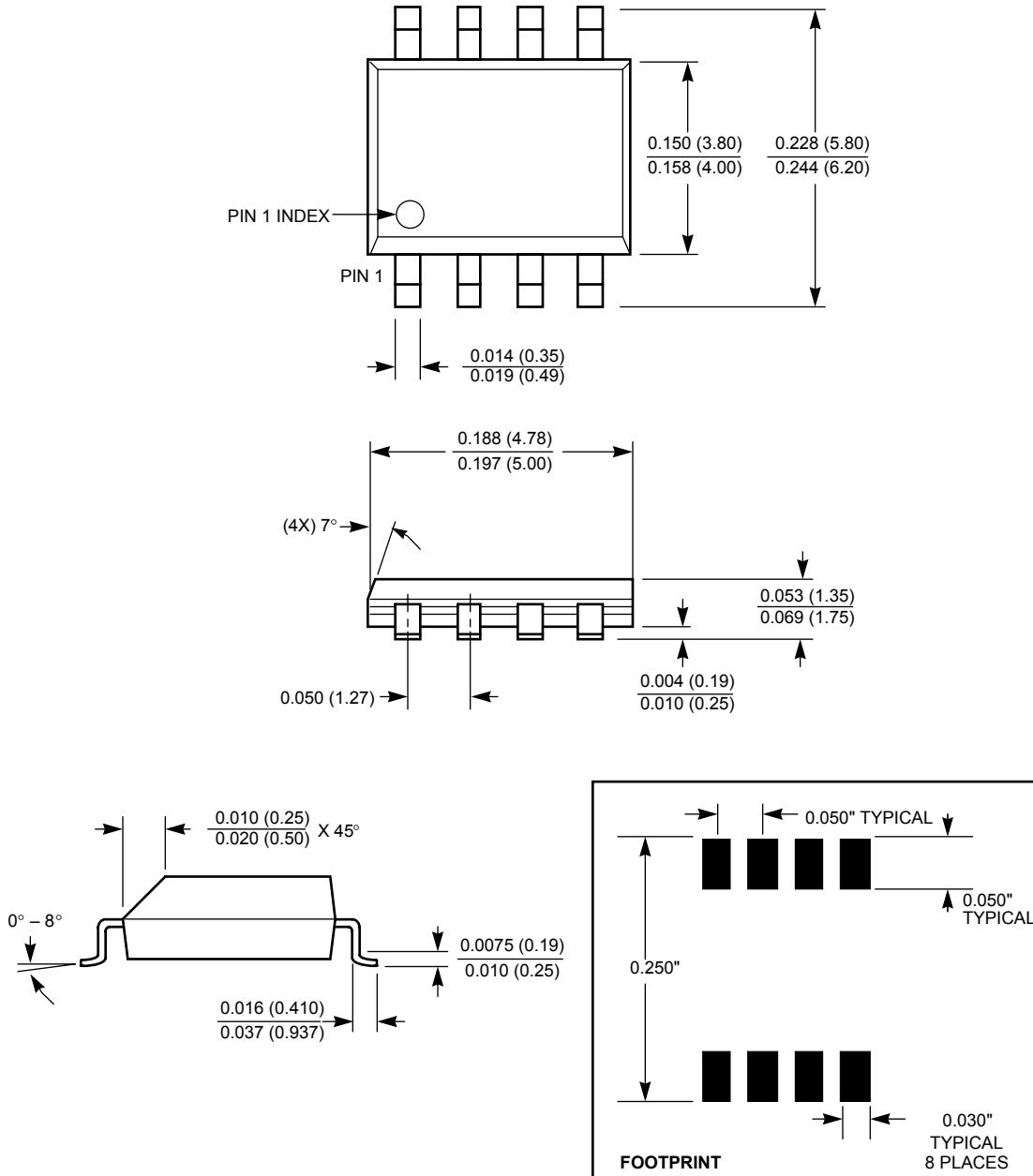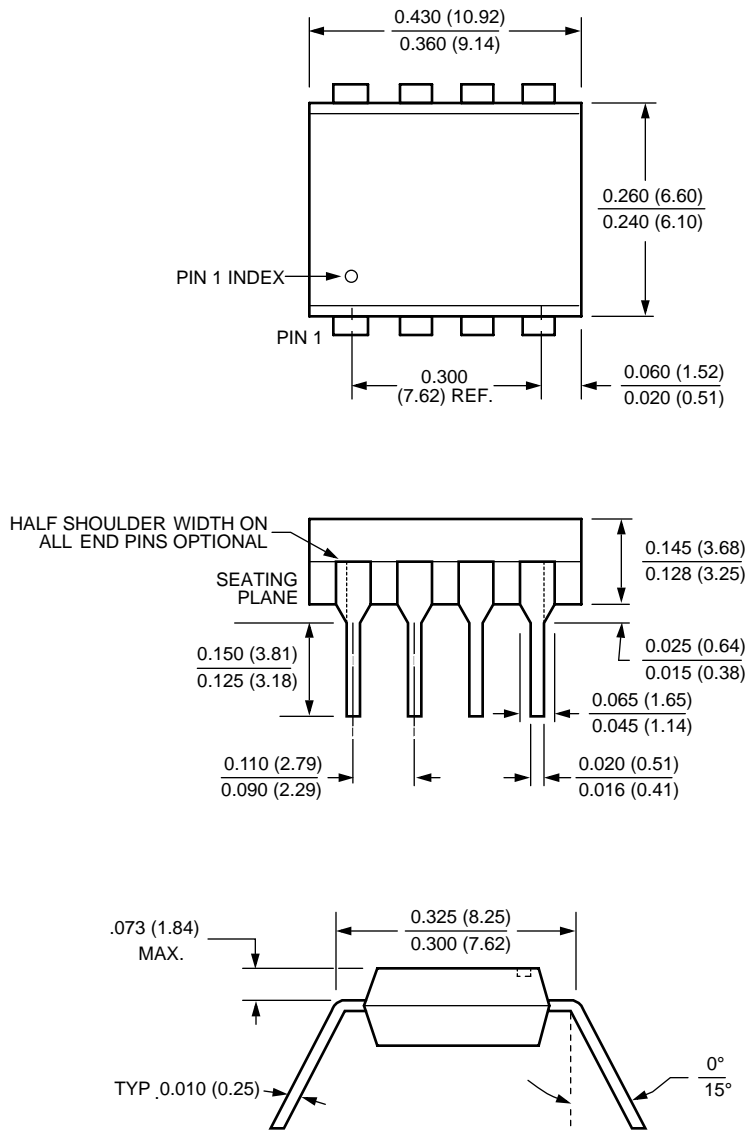**t$_{WDO}$ vs. Voltage/Temperature (WD1,0 0=0,1)**
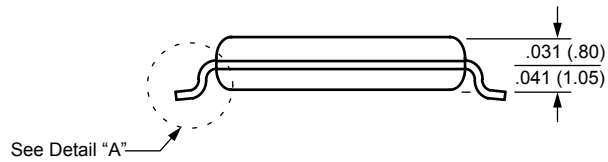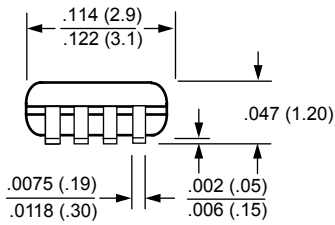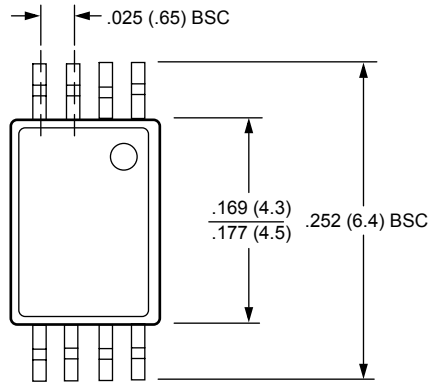
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

PIN 1 INDEX →

PIN 1

$\frac{0.150\ (3.80)}{0.158\ (4.00)}$ $\frac{0.228\ (5.80)}{0.244\ (6.20)}$

$\frac{0.014\ (0.35)}{0.019\ (0.49)}$

$\frac{0.188\ (4.78)}{0.197\ (5.00)}$

(4X) 7°

$\frac{0.053\ (1.35)}{0.069\ (1.75)}$

0.050 (1.27) →

$\frac{0.004\ (0.19)}{0.010\ (0.25)}$

$\frac{0.010\ (0.25)}{0.020\ (0.50)}$ X 45°

0° – 8°

$\frac{0.0075\ (0.19)}{0.010\ (0.25)}$

$\frac{0.016\ (0.410)}{0.037\ (0.937)}$

0.050" TYPICAL

0.050" TYPICAL

0.250"

0.030" TYPICAL
8 PLACES

FOOTPRINT

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

$$\frac{0.430\ (10.92)}{0.360\ (9.14)}$$

$$\frac{0.260\ (6.60)}{0.240\ (6.10)}$$

PIN 1 INDEX

PIN 1

$$\frac{0.300}{(7.62)\ REF.}$$

$$\frac{0.060\ (1.52)}{0.020\ (0.51)}$$

HALF SHOULDER WIDTH ON
ALL END PINS OPTIONAL

SEATING
PLANE

$$\frac{0.145\ (3.68)}{0.128\ (3.25)}$$

$$\frac{0.150\ (3.81)}{0.125\ (3.18)}$$

$$\frac{0.025\ (0.64)}{0.015\ (0.38)}$$

$$\frac{0.065\ (1.65)}{0.045\ (1.14)}$$

$$\frac{0.110\ (2.79)}{0.090\ (2.29)}$$

$$\frac{0.020\ (0.51)}{0.016\ (0.41)}$$

.073 (1.84)
MAX.

$$\frac{0.325\ (8.25)}{0.300\ (7.62)}$$

TYP .010 (0.25)

$$\frac{0°}{15°}$$

NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V

.025 (.65) BSC

$\dfrac{.169\ (4.3)}{.177\ (4.5)}$ .252 (6.4) BSC

$\dfrac{.114\ (2.9)}{.122\ (3.1)}$

.047 (1.20)

$\dfrac{.0075\ (.19)}{.0118\ (.30)}$ $\dfrac{.002\ (.05)}{.006\ (.15)}$

.010 (.25)

Gage Plane

Seating Plane

0° − 8°

$\dfrac{.019\ (.50)}{.029\ (.75)}$

Detail A (20X)

$\dfrac{.031\ (.80)}{.041\ (1.05)}$

See Detail "A"
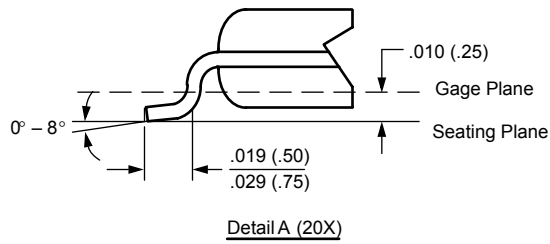
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X5083

Ordering Information

Vcc Range	V$_{TRIP}$ Range	Package	Operating Temperature Range	PART NUMBER $\overline{RESET}$ (Active LOW)
4.5-5.5V	4.5.4.75	8 pin PDIP	0ºC - 70ºC	X5083P-4.5A
		8L SOIC	0ºC - 70ºC	X5083S8-4.5A
			-40ºC - 85ºC	X5083S8I-4.5A
4.5-5.5V	4.25.4.5	8 pin PDIP	0ºC - 70ºC	X5083P
		8L SOIC	0ºC - 70ºC	X5083S8
			-40ºC - 85ºC	X5083S8I
		8L TSSOP	0ºC - 70ºC	X5083V8
2.7-5.5V	2.85-3.0	8L SOIC	0ºC - 70ºC	X5083S8-2.7A
			-40ºC - 85ºC	X5083S8I-2.7A
		8L TSSOP	0ºC - 70ºC	X5083S8-2.7A
2.7-5.5V	2.55-2.7	8L SOIC	0ºC - 70ºC	X5083S8-2.7
			-40ºC - 85ºC	X5083S8I-2.7A
		8L TSSOP	0ºC - 70ºC	X5083V8-2.7
1.8-3.6V	1.7-1.8	8L SOIC	0ºC - 70ºC	X5083S8-1.8
		8L TSSOP	0ºC - 70ºC	X5083V8-1.8

Part Mark Convention

8-Lead TSSOP

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┌─────────┐
│  EYWW   │
│  XXXXX  │
└─────────┘
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583AG = 1.8 to 3.6V, 0 to +70°C, V_{TRIP}=1.7-1.8V
583AH = 1.8 to 3.6V, -40 to +85°C, V_{TRIP}=1.7-1.8V
583F = 2.7 to 5.5V, 0 to +70°C, V_{TRIP}=2.55-2.7V
583G = 2.7 to 5.5V, -40 to +85°C, V_{TRIP}=2.55-2.7V
583AN = 2.7 to 5.5V, 0 to +70°C, V_{TRIP}=2.85-3.0V
583AP = 2.7 to 5.5V, -40 to +85°C, V_{TRIP}=2.85-3.0V
X583 = 4.5 to 5.5V, 0 to +70°C, V_{TRIP}=4.25-4.5V
583I = 4.5 to 5.5V, -40 to +85°C, V_{TRIP}=4.25-4.5V
583AL = 4.5 to 5.5V, 0 to +70°C, V_{TRIP}=4.5-4.75V
583AM = 4.5 to 5.5V, -40 to +85°C, V_{TRIP}=4.5-4.75V

YWW = year/work week device is packaged.

8-Lead SOIC/PDIP

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┌─────────────┐
│ X5083/85 X  │
│      XX     │
└─────────────┘
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AG = 1.8 to 3.6V, 0 to +70°C, V_{TRIP}=1.7-1.8V
AH = 1.8 to 3.6V, -40 to +85°C, V_{TRIP}=1.7-1.8V
F = 2.7 to 5.5V, 0 to +70°C, V_{TRIP}=2.55-2.7V
G = 2.7 to 5.5V, -40 to +85°C, V_{TRIP}=2.55-2.7V
AN = 2.7 to 5.5V, 0 to +70°C, V_{TRIP}=2.85-3.0V
AP = 2.7 to 5.5V, -40 to +85°C, V_{TRIP}=2.85-3.0V
Blank = 4.5 to 5.5V, 0 to +70°C, V_{TRIP}=4.25-4.5V
I = 4.5 to 5.5V, -40 to +85°C, V_{TRIP}=4.25-4.5V
AL = 4.5 to 5.5V, 0 to +70°C, V_{TRIP}=4.5-4.75V
AM = 4.5 to 5.5V, -40 to +85°C, V_{TRIP}=4.5-4.75V